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# Datasheet for the decision of 14 June 2007

**Case Number:** T 1409/04 - 3.5.04

**Application Number:** 94931904.0

**Publication Number:** 0683955

**IPC:** H04N 5/907

**Language of the proceedings:** EN

**Title of invention:**
Management of channel buffer in video decoders

**Patentee:**
LSI Logic Corporation

**Opponent:**
Interessengemeinschaft für Rundfunkschutzrechte e.V. (IGR e.V.)

**Headword:**
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**Relevant legal provisions:**
EPC Art. 54, 56

**Keyword:**
"Examination of opposition - burden of proof on the opponent"

**Decisions cited:**
-

**Catchword:**
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Beschwerdekammern | Boards of Appeal | Chambres de recours

**Case Number:** T 1409/04 - 3.5.04

# D E C I S I O N
**of the Technical Board of Appeal 3.5.04**
**of 14 June 2007**

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| **Appellant:** (Opponent) | Interessengemeinschaft für Rundfunkschutzrechte e.V. (IGR e.V.)<br>Bahnstraße 62<br>DE-40210 Düsseldorf (DE) |
| **Representative:** | Eichstädt, Alfred<br>Maryniok & Partner<br>Kuhbergstraße 23<br>DE-96317 Kronach (DE) |
| **Respondent:** (Patent Proprietor) | LSI Logic Corporation<br>1551 McCarthy Boulevard<br>Milpitas<br>CA 95035 (US) |
| **Representative:** | Hallam, Arnold Vincent<br>Marks & Clerk<br>144 New Walk<br>Leicester LE1 7JA (GB) |
| **Decision under appeal:** | **Decision of the Opposition Division of the European Patent Office posted 19 October 2004 rejecting the opposition filed against European patent No.0683955 pursuant to Article 102(2) EPC.** |

**Composition of the Board:**

**Chairman:** F. Edlinger
**Members:** C. Kunzelmann
T. Karamanli

## Summary of Facts and Submissions

I. The appeal is against the decision of the opposition division to reject the opposition against European patent No. 0 683 955.

II. The independent claims 1 and 13 of the opposed patent read as follows.

Claim 1:

"A video decoding system comprising:
buffer means (20) for buffering a video bitstream received from a fixed rate transmission channel (21) said bitstream including picture data;
reconstructing means (30), coupled to said buffer means, for reconstructing pictures from said picture data, said picture data being transferred from said buffer means to said reconstructing means when said buffer means receives all of said picture data belonging to one single picture;
display control means (32), coupled to said reconstructing means, for controlling the display of said reconstructed pictures; and
controller means (36) for controlling said reconstructing means and said display control means;
characterised in that said controller means (36) is arranged to synchronize said reconstructing means (30) with said display control means (32)."

Claim 13:

"A process of decoding a video bitstream comprising the steps of:

receiving a video bitstream including picture data at a fixed rate;
storing all of the picture data for a single picture in a channel buffer;
decoding said single picture data when all of said single picture data has been received by said channel buffer;
reconstructing an image from said single picture data; and
controlling the rate of a display controller in response to a rate of picture reconstruction, said display controller generating video output signals representative of said reconstructed picture."

III. The decision under appeal referred in the reasons to document

D1: EP 0 431 319 A2

and can be summarised as follows.

D1 disclosed the features of the precharacterising portion of claim 1. However, the feature of the characterising portion of claim 1 was not explicitly mentioned in D1. Nor could this feature be "plainly or logically" derived from D1 in an obvious manner. The problem solved by the system of claim 1 could be regarded as how to create a decoding system of compressed video with a fixed input rate so that data losses in the picture reconstruction/decoding chain were avoided. A combination of D1 with the common general knowledge of a skilled person would not inevitably lead to the claimed invention because D1 remained silent as to the functionality of the control

signal "j" in figure 4 of D1. The signal "j" could serve many different purposes which did not necessarily relate to a synchronisation between the decoder (or equivalent reconstructing means) and the frame memory (or equivalent display control means). It could, for instance, provide information about decoder readiness, an active data transfer period, sizing or storage location for the frame memory, etc. Starting from D1, a person skilled in the art could come to quite a number of different solutions to the problem solved by the system of claim 1 without selecting the claimed solution. D1 did not contain clear synchronisation requirements. The switching between frame memory areas for display purposes and the filling of frame memory areas with decoded data might be completely decoupled. D1 left open how the interaction between the decoding unit and the frame memory was performed.

Claim 13 specified method steps which were substantially equivalent to the system features of claim 1.

IV. The appellant's (opponent's) arguments can be summarised as follows.

The subject-matter of claims 1 and 13 was not new with respect to D1. At least, it did not involve an inventive step having regard to D1 in conjunction with the common general knowledge of a person skilled in the art.

Both D1 and the opposed patent related to a decoding system where the receiving buffer continuously received a video bitstream so that, when a picture was read out

from the buffer memory, the next picture could already have been completely read in, depending on the data rates of the reading in and the reading out of the buffer memory.

Although D1 (page 6, line 30, to page 7, line 10) did not explicitly disclose the feature of the characterising portion of claim 1, it was implicit that the reconstructing and display means had to be synchronized. At least such a synchronisation was obvious to a person skilled in the art. In D1 a controller 40 triggered the reconstructing means 38. The picture was reconstructed and then written into a first area of a frame memory 39 in the receiver, but read out from a second area of the frame memory 39 and then outputted to a monitor or the like. Thus the two areas of the frame memory necessarily had to be operated in a push-pull manner and the signal "j" could reasonably only be a switch over signal for alternating the functions of the two areas when simultaneously reading in image data in one area and reading out data from the other area. This switching necessarily had to be synchronised with the control of the reconstructing means for two reasons. Namely overwriting of the content of a frame memory area which had not yet been read had to be avoided, and access conflicts occurring if data were simultaneously written into and read from one frame memory area had to be avoided. It became even more evident that signal "j" was a switch over signal if the inverse process to the decoding and outputting of pictures was considered, namely the operation of the frame memory 31 on the transmitter side of the transmission channel in D1. This memory also had two areas, one for reading in an image from a camera and

one for reading out a read image and transferring it to a coding unit 32. The signal "a" for controlling the frame memory 31 was explicitly disclosed as a switch over signal determining which of the two frame memory areas was used for which of the two purposes, respectively (D1, page 6, lines 32 to 34).

These arguments also applied to claim 13.

V. The respondent's (patent proprietor's) arguments can be summarised as follows.

Concerning the precharacterising portion of claim 1, it was acknowledged that when the receiver buffer in D1 was empty, the controller 40 waited until a first full frame was received before outputting the initial decoding signal. However when a stream of data was received the buffer filled up with a plurality of frames, thus requiring a large receiver buffer, as discussed in paragraph [0037] of the patent specification with reference to a conventional channel buffer management scheme. In contrast, the buffer of the opposed patent never contained data relating to a plurality of pictures because picture data were transferred from the buffer means to the reconstructing means when (meaning: as soon as) said buffer means received all of said picture data belonging to one single picture. Therefore the amount of memory allocated to the buffer could be substantially reduced. Thus claim 1 was inventive (and hence novel) already for this reason.

Concerning the characterising portion of claim 1, the appellant's arguments betrayed a misunderstanding of

the term "synchronize". A dictionary definition of this term was "to operate simultaneously". Thus synchronisation of the reconstructing means with the display control means required substantially simultaneous operation of the two constituent parts. Such simultaneous operation was clearly illustrated in figure 5 of the patent. A skilled person would understand synchronous operation to correspond to the synchronisation of video output signals with the reconstruction of incoming picture data by the reconstructing means, as clearly supported by the description and claim 13 of the patent. The novel features of the precharacterising and characterising portions of claim 1 solved the problems of "how to create a decoding system in which the receiver buffer size is minimised and in which overflow errors are avoided", and "how to create a decoding system of compressed video with a fixed input rate so that data losses in the picture reconstructing/decoding chain are avoided", respectively.

It was not implicit from D1 that the signal "j" was a switch over signal. Even if it were, it would inherently be applied asynchronously with decoder activation and it would not necessarily lead to synchronisation as a skilled person would understand it. Moreover the mere application of a control signal to the frame memory at the same time as the decoding unit activates would not necessarily result in synchronous operation of the reconstructing means and the display control means. In D1 overwriting of the content of a frame memory area which had not yet been read could be avoided if each storage region were sufficiently large to take multiple frames. The fact that signal "a" used

by the transmitter was a switch over signal did not lead to the conclusion that signal "j" used by the receiver had to be a switch over signal. Signal "a" could be issued in dependence upon an occupied information area signal "f" for which there was no equivalent on the receiver side. The system of D1 was designed to asynchronously operate the transmitter and the receiver and directed at solving a problem associated with meeting a requirement inherent to asynchronous systems (see D1, page 4, lines 7 to 9).

Similar arguments applied to claim 13 in which the rate of the display controller was clearly linked to be synchronised with that of the reconstructing means.

Furthermore the respondent submitted that the appellant had not provided any arguments or supporting evidence which would support an objection as to lack of inventive step. Moreover both the examining division and the opposition division had found that the invention as claimed in the patent was both novel and inventive when viewed against D1.

VI. The appellant requested in writing that the decision be set aside and the patent be revoked, and the respondent requested in writing that the appeal be dismissed. Both parties requested oral proceedings as auxiliary requests.

VII. With a communication dated 21 February 2007 and annexed to the summons to oral proceedings, the board indicated that it appeared that only two features were disputed between the parties, namely

(a) "said picture data being transferred from said buffer means to said reconstructing means when said buffer means receives all of said picture data belonging to one single picture" and

(b) "said controller means (36) is arranged to synchronize said reconstructing means (30) with said display control means (32)".

Concerning feature a), the board indicated that the disclosure of D1, page 6, line 56, to page 7, line 10, in particular the situation relating to the controller 40 waiting until a full frame was received before outputting the decoding start signal appeared to be relevant.
Concerning feature b), the board indicated that the correct construction and relevance of the term "synchronize" in the context of the claims would have to be discussed, in particular whether it was correctly construed in the sense given it by the respondent ("operate simultaneously").

VIII. In response to the board's communication, both the appellant and the respondent announced that they would not attend the oral proceedings. The appellant maintained the request for revocation of the patent essentially for the reasons given in the statement of grounds of appeal, and the respondent did not submit any further requests or arguments.

IX. Oral proceedings were held in the absence of the duly summoned parties on 14 June 2007 in accordance with Rule 71(2) EPC. At the end of the oral proceedings the board announced its decision.

## Reasons for the Decision

1. The appeal is admissible.

2. *Novelty (Articles 100(a) and 54 EPC)*

2.1 According to the established case law (see "Case Law of the Boards of Appeal of the European Patent Office", 5th edition 2006, I.C.2.1), for an invention to lack novelty within the meaning of Article 54(1) EPC its subject-matter must be directly and unambiguously derivable from the prior art.

2.2 In the present case both parties agree with the decision under appeal that D1 does not explicitly disclose the feature of the characterising portion of claim 1, and the board concurs with this. The board also concurs with the argument used both in the decision under appeal and in the respondent's reply, that the signal "j" in D1 is not necessarily a switch over signal, but could serve other purposes not necessarily relating to a synchronisation between the decoder and the frame memory. The appellant's arguments in this context do not take into account that other meanings of the signal "j" are possible, such as those mentioned in the decision under appeal.

2.3 Even if signal "j" (cf D1, page 7, lines 8 to 10 and figure 4) were a control signal switching the frame memory 39 from a first area (into which the decoded video signal is written) to a second area (used for reading out the decoded video data), it would still be

possible that each area would be sufficiently large to take multiple frames of data. Then, each data frame could be output (to a display) from its area of frame memory **asynchronously** with the input of data frames from the reconstructing means to the other area, similar to the asynchronous data transfer of frame data to and from the receiver buffer, which is also large enough to be filled up with a plurality of frames. In these respects D1 is totally silent.

2.4 Both parties agree with the decision under appeal that the arguments brought forward in respect of claim 1 also apply to the process of decoding a video bitstream of claim 13. The board concurs with this view. D1 at least does not disclose the feature "controlling the rate of a display controller in response to a rate of picture reconstruction".

2.5 In the board's view therefore the subject-matter of claims 1 and 13 is not directly and unambiguously derivable from D1. Thus the board judges that the subject-matter of claims 1 and 13 is new within the meaning of Article 54(1) EPC, so that the ground for opposition of lack of novelty (Articles 100(a) and 54(1) EPC) does not prejudice the maintenance of the patent.

3. *Inventive step (Articles 100(a) and 56 EPC)*

3.1 The appellant's submissions as to inventive step are largely identical to those as to novelty. In particular the same evidence (namely document D1) is relied upon, and the feature of the characterising portion of claim 1 is considered to be implicit in D1 or at least obvious having regard to D1 in conjunction with the

common general knowledge of a person skilled in the art. However the appellant did not provide any arguments as to why the feature of the characterising portion of claim 1 was obvious having regard to D1 in conjunction with the common general knowledge of a person skilled in the art. The appellant neither provided any evidence for the alleged common general knowledge, even though the respondent had stressed the point that such arguments and evidence were lacking. In the absence of any indication of what the allegedly relevant common general knowledge is, and in the absence of any evidence therefor, the board considers the objection as to lack of inventive step to be a mere allegation. In accordance with established case law (see "Case Law of the Boards of Appeal of the European Patent Office", 5th edition 2006, VI.K.5.1.1 and VI.K.5.1.2(b)) an opponent who alleges facts which could disprove the existence of an inventive step bears the burden of proof in this respect. Thus the lack of evidence for the alleged common general knowledge weighs against the appellant.

3.2 Furthermore, the appellant submitted the argument that it was even more evident ("noch offensichtlicher") in D1 that signal "j" was a switch over signal when the inverse process on the transmitter side was taken into consideration. However the appellant did not provide any argumentation as to why or how the process on the transmitter side determines the process on the receiver side. In this respect the board concurs with the respondent's argument that the signal "a" used on the transmitter side could be issued in dependence on an occupied information area signal "f" for which there is no equivalent on the receiver side. Thus signal "j"

need not be a switch over signal in analogy to the "area switching control signal (a)" which "indicates whether the first area or the second area should be used" (see D1, page 6, lines 30 to 34). The board therefore does not see how the considerations of the process on the transmitter side prove the allegation that the subject-matter of claims 1 and 13 lacks an inventive step.

3.3 Since the board has not been convinced by the facts, evidence and arguments submitted by the appellant, the appeal has to be dismissed.

## Order

## For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

D. Sauter F. Edlinger