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D E C I S I O N
of 1 June 2006

Case Number: T 1094/04 - 3.4.03

Application Number: 99122317.3

Publication Number: 1001462

IPC: H01L 23/498

Language of the proceedings: EN

Title of invention:

Semiconductor device with connection terminals in the form of a grid array

Applicant:

NEC Electronics Corporation, et al

Opponent:

-

Headword:

-

Relevant legal provisions:

EPC Art. 54, 56

Keyword:

"Novelty (yes)"
"Inventive step (yes)"

Decisions cited:

-

Catchword:

-



Case Number: T 1094/04 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 1 June 2006

Appellant: NEC Electronics Corporation
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Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 24. March 2004
refusing European application No. 99122317.3
pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: R. G. O'Connell
Members: V. L. P. Frank
T. Bokor

Summary of Facts and Submissions

- I. This is an appeal from the refusal of European patent application 99 122 317.3 for lack of novelty (Article 54 EPC).
- II. In oral proceedings before the board the appellant applicant filed amended claims and description.

Claim 1 is now worded as follows:

"A semiconductor device with an IC chip provided on one face of a substrate (1), wherein a plurality of connection terminals (106) are provided on the other face of said substrate, are electrically connected to said IC chip (101, 102) through electrical connecting devices, form a rectangular grid array, and are arranged in positions other than corners of the array, characterized in that reinforcement terminals (401) are provided outside the grid array on the same face as the connection terminals, and at least one of said reinforcement terminals is an index terminal (400) for indicating a direction of the semiconductor device, said index terminal is not electrically connected and said index terminal is provided asymmetrically."

Claims 2 to 12 are dependent on claim 1.

III. The following prior art documents *inter alia* were cited in the examination procedure:

D2: JP 10092965 A

D4: US 5796169 A

D5: JP 01217931 A

D6: JP 08046313 A

Computer generated translations of documents D2 and D6 (obtained online from the Industrial Property Digital Library of Japan, <http://www4.ipdl.ncipi.go.jp/Tokujitu/tjsogodbenk.ipdl>) were sent to the appellant applicant by the board as an annex to the summons to oral proceedings.

IV. In the decision under appeal the examining division found that the semiconductor device of claim 1 lacked novelty over document D4. In their view, this document disclosed a rectangular grid array of connection terminals with reinforcement terminals provided outside this array, as it was possible to identify many subsets of connection terminals satisfying this requirement and also the requirement that the corner positions of the array were not occupied. The feature "an index terminal ... for indicating a direction of the semiconductor device" was interpreted as a terminal being suitable for this purpose, even if this use had not been indicated in the prior art. The asymmetric reinforcement terminals shown in Figure 3 of D4 were, however, suitable for the purpose of indexing.

V. The appellant applicant argued essentially as follows:

- The aim of the invention was to provide a semiconductor device which reliably connected the connection terminals to a mount board, reduced thermal and mechanical stress on the connection terminals and allowed easy indexing of the direction of the semiconductor device. This was achieved by using one of the reinforcement terminals as indexing terminal by locating it asymmetrically on the substrate. This dual function of one of the terminals (ie reinforcement and indexing) was not rendered obvious by the prior art.

VI. The appellant applicant requests that the decision under appeal be set aside and that a patent be granted in the following version:

Claims: 1 to 12 filed at the oral proceedings

Description: pages 1 to 4, 4a, 5 to 18 filed at the oral proceedings

Drawings: as originally filed.

Reasons for the Decision

1. The appeal is admissible.
2. *Amendments (Article 123(2) EPC)*

No objections in this respect were raised during the examination procedure.

Claim 1 now specifies that "said index terminal is provided asymmetrically". This is the same wording as used in the description as originally filed (column 7, lines 20 to 22 of the published application).

The description has been adapted to the claims and the prior art acknowledged.

The board is therefore satisfied that Article 123(2) EPC is not contravened.

3. *Novelty (Article 54 EPC)*

3.1 Claim 1 is directed to a semiconductor device comprising an integrated circuit (IC) mounted on one face of a substrate. Connection terminals 106 in the form of solder balls are provided on the other face of the substrate. This kind of connection system is called a ball grid array (BGA). The connection terminals form a rectangular grid array of which the corners are left free, since it has been found that thermal and mechanical stress render these corner positions less reliable for electrical connections. Reinforcement terminals 401 are provided outside the rectangular array. At least one of these reinforcement terminals is used as index terminal 400 for indicating the orientation of the semiconductor device by locating it asymmetrically on the substrate (Figs 4 to 7).

3.2 Document D4 discloses a BGA package in which support solder is added to the array where necessary to provide both structural reinforcement and thermal conduction (Abstract). L-shaped patterns of high melting

temperature support solder, with a cross section analogous to the solder balls, are formed in the corners of the substrate, although other shapes and other locations on the substrate can be employed consistent with the premise that the cross section of the structure along one axis of the array is analogous to that of a solder ball (column 2, lines 45 to 53). In Figure 3 different shapes and possible locations on the substrate of the reinforcement structures are shown. Symmetric and asymmetric structures may be used, allowing the designer flexibility in placing the support solder for achieving maximal structural integrity (column 5, lines 12 to 15). In particular, an asymmetric support structure in the form of a lower case "h" is shown at the lower right hand portion of Figure 3, although no particular relevance of this pattern is disclosed in the text of this document.

- 3.3 The board, however, cannot identify in the structure disclosed in Figure 3 of D4 any subset of connection terminals which would satisfy the requirements of claim 1 that the connection terminals form a rectangular grid of which the corner positions are left free and having reinforcement terminals located outside this array, contrary to the assertion by the examining division in the decision under appeal at point 4.i of the reasons. Clearly all the reinforcement terminals lie within the boundary of the rectangular grid array; in fact reinforcement terminals 16 to 18 lie exactly at the corner positions of the grid array as a whole. When a rectangular subset of the grid array shown in Figure 3 is considered, then either the corners of this subset are not free of connection terminals or the reinforcement terminals are located at the corners of

- this subset and not outside its area. In neither case are the requirements of claim 1 fulfilled.
- 3.4 Document D2 on the other hand discloses a BGA in which the solder balls at the corners are dummy balls not connected to the IC chip, since deformation of the semiconductor package may result in disconnection of these solder balls. The corner solder balls are therefore used as reinforcement terminals within the meaning of the present invention. It is further mentioned in this document that reinforcement terminals were conventionally provided outside the array of terminals, but that the arrangement disclosed in this document reduced the overall area of the semiconductor package ([0006] and [0026]). The determination of the orientation of the semiconductor package is not addressed in this document.
- 3.5 Only the somewhat unclear English abstract of document D5 was available to the board. It discloses a semiconductor package in which the corner positions of the rectangular BGA are left free. Additional "alignment/reliability-mounting bumps 4a, 4b" are provided at the four corners of the BGA, ie within the rectangular area of the array. Although further bumps 4c which appear to lie outside the area of the rectangular BGA are shown in Figure 1, their function is not addressed in the abstract.
- 3.6 Document D6 discloses a semiconductor package in which a BGA 4 is surrounded by additional dummy bumps 10 provided outside the array and at the corner positions of the package. The additional bumps 10 are, however, not foreseen as reinforcement terminals but as spacers

for preventing a barrel shape deformation of the solder balls of the BGA during the melting/mounting step of the package (Figures 1 and 5 and [0005]). The determination of the orientation of the semiconductor package is also not addressed in this document.

3.7 It follows from the above that the semiconductor device of claim 1 is new having regard to the available prior art.

4. *Inventive step (Article 56 EPC)*

4.1 The appellant applicant has argued that it was the gist of the invention to recognize that one of the reinforcement terminals could be used simultaneously for determining the mounting orientation of the semiconductor package, ie its use as an indexing terminal, by providing it asymmetrically on the substrate. BGAs have conventionally been designed symmetrically and it would not be obvious to the skilled person to break this symmetry.

4.2 The examining division argued at point 8 of the decision under appeal that document D6 disclosed reinforcement terminals located outside the area of the BGA. That this is not so has already been mentioned above at point 3.6. This document is therefore not a reasonable starting point for assessing inventive step.

4.3 Although document D2 discloses that reinforcement terminals were conventionally provided outside the area of the BGA (see point 3.4), it underlines the benefits achieved by locating the reinforcement terminals at the corners of this area, ie reduction of the area of the

semiconductor package. Hence it teaches away from reverting to the previous approach of providing reinforcement terminals outside the grid array. The same can be said of the arrangements disclosed in documents D4 and D5, where the reinforcement terminals are provided at the corner positions of, or within the grid array.

- 4.4 None of the available prior art documents address the issue of determining the orientation of the semiconductor package. Although the lower case "h" reinforcement terminal disclosed in Figure 3 of document D4 could be used for this purpose by virtue of its asymmetric form and location, there is no related disclosure in D4. In fact D4 is concerned with a completely different problem, namely to adapt the cross section of the reinforcement terminals to that of the solder balls in order to reduce the differential wetting which occurs when mounting them on a circuit board as a result of their differing shapes (column 1, line 66 to column 2, line 11). It is therefore pure speculation that the skilled person reading document D4 would have recognized that the particular lower case "h" reinforcement terminal depicted only in the figure was suitable for indicating the orientation of the semiconductor package.
- 4.5 Therefore, the skilled person would find no specific suggestion or motive to transfer the asymmetric shape of the h-shaped reinforcement terminal of document D4 to a position outside the grid array as required by claim 1 of the present application. This is all the more so, as the solution proposed in D4 relates to reinforcement terminals which are within the grid array,

and having solder structures with dimensions compatible with the shape of the solder balls of the grid array; see point 3.2 above.

- 4.6 For the foregoing reasons the board concludes that providing a reinforcement terminal asymmetrically on the substrate so that it fulfils the double function of reinforcement and indication of the orientation of the semiconductor device is not rendered obvious by the prior art available. The semiconductor device of claim 1 is therefore considered as involving an inventive step within the meaning of Article 56 EPC.
5. Hence the board judges that the application fulfils the requirements of the EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

Claims: 1 to 12 filed at the oral proceedings

Description: pages 1 to 4, 4a, 5 to 18 filed at the oral proceedings

Drawings: as originally filed.

Registrar

Chair

S. Sánchez Chiquero

R. G. O'Connell