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Datasheet for the decision of 16 November 2006

Case Number: T 1093/04 - 3.5.02

Application Number: 94119510.9

Publication Number: 0657854

IPC: G07B 17/02

Language of the proceedings: EN

Title of invention:
Programmable clock module for postage metering control system

Patentee:
PITNEY BOWES INC.

Opponents:
NEOPOST LTD
Francotyp-Postalia Aktiengesellschaft & Co. KG

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - main request - (yes)"

Decisions cited:
T 0005/81

Catchword:
-

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Case Number: T 1093/04 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 16 November 2006

Appellant: (Opponent 01)	NEOPOST LTD South Street Romford, Essex, RM1 2AR (GB)
Representative:	Weinmiller, Jürgen Spott, Weinmiller & Böhm Patentanwälte Lennéstrasse 9 D-82340 Feldafing (DE)
Former Opponent 02	Francotyp-Postalia Aktiengesellschaft & Co. KG Triftweg 21-26 D-16547 Birkenwerder (DE)
Respondent: (Patent Proprietor)	PITNEY BOWES INC. World Headquarters One Elmcroft Stamford, CT 06926-0700 (US)
Representative:	Avery, Stephen John Hoffmann Eitle Patent- und Rechtsanwälte Arabellastrasse 4 D-81925 München (DE)
Decision under appeal:	**Decision of the Opposition Division of the European Patent Office posted 26 July 2004 rejecting the opposition filed against European patent No. 0657854 pursuant to Article 102(2) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: J.-M. Cannard
P. Mühlens

Summary of Facts and Submissions

I. Opponent 01 appealed against the decision of the opposition division rejecting the opposition filed against European patent No. 0 657 854.

II. Prior art documents:

D1: DE-A-30 40 352, and

D4: US-A-5 097 437,

considered during the proceedings before the opposition division remain relevant to the present appeal.

III. Claim 1 of the patent in suit as granted, maintained on appeal as main request, reads as follows:

"An electronic postage meter control system having:

a printing means having a plurality of prime movers (552) for printing of a postage indicia in response to a control circuit;

a programmable microprocessor (13) in bus communication with

an accounting means having memory units (MU) for accounting for said postage printed by said printing means;

program memory means for generating data; and

an integrated circuit (15);

characterised by:

said data including timing data;

said integrated circuit (15) having an address decoding module (20) for generating a unique combination of control signals in response to a respective address placed on said bus by said microprocessor (13);

timer registers responsive to ones of said control signals from said address decoding module (20) to enable writing of said timing data into said timer registers by said microprocessor (13); and

timer means (600) responsive to said timing data for generating one of a plurality of timing signals."

IV. Oral proceedings were held on 16 November 2006.

V. The arguments of the appellant opponent 01 can be summarized as follows:

Claim 1 of the main request was essentially concerned with the solution to the problem of matching the ASIC (Application Specific Integrated Circuit) clock rate to that of the microprocessor in an electronic postage meter control system. The problem of interfacing microprocessors with ASIC modules was generally well known, for instance from document D4, and not specific to a postage meter system.

D4, which disclosed a control unit (100) for controlling a microcomputer system, was the starting

point for the assessment of inventive step. In D4, the control unit comprised a system controller (50) which was an ASIC module and provided timing signals for all the subsystems of the microcomputer so that it could accept faster processors and memories while incorporating slower bus technology and slower peripheral and accessory devices.

It would have been obvious to the skilled person to apply the solution disclosed in D4 to a postage meter control system in order to match its ASIC clock rate to that of the system microprocessor. Whether the programmable array logic circuits (52, 53) of D4 were, or were not, address decoding modules disposed within an ASIC module (50), was irrelevant for assessing inventive step.

The meaning of the expressions "program memory means" and "address decoding module" in claim 1 was very broad. The description and figure 1 of the patent in suit, according to which the system processor provided control signals for writing appropriate data into the timer registers, did not support the function of the claimed address decoding module. The control unit of D4, in which the processor provided a unique combination of control signals for selecting timing and clock signals, anticipated the integrated circuit specified in claim 1.

It was obvious to the skilled person at the patent priority date to implement the logical functions of the control system of the postage meter described in document D1 as an ASIC module.

VI. The arguments of the respondent proprietor can be summarized as follows:

The skilled person wishing to make a control system for a postage meter system would not start from D4. D4 was concerned with a microcomputer and with the particular timing problems which arose when its processor, memories and peripheral devices had different working frequencies. This problem and its solution, which was to control the frequency clock of the system processor of D4, were different from the problem addressed by the invention and its solution, which was to match the clock of the ASIC module of the postage meter control system.

The conventional franking machine according to the prior art comprised three types of integrated circuits: a microprocessor, an ASIC module and memory means. The idea at the basis of the invention was to have only one generic ASIC module that could work with microprocessors having different working frequencies. Upon power-up of the system, data stored in program memory means and representing the microprocessor speed were written by an address decoding module into timer registers and used in timer means for generating a matched clock rate for the ASIC module. Considering the teaching of D4, where an ASIC module set the appropriate frequency for the microprocessor, the skilled person would not arrive at the claimed invention.

The postage meter described in D1 was a system according to an old technology in which three modules, a control system, printing means and accounting means,

each having its own microprocessor with its own clock, were used. No address bus was necessary and the control system worked in an independent manner. Starting from D1, two steps were necessary for the skilled person to arrive at the claimed control system: firstly changing the whole structure of D1 to accommodate an ASIC module, secondly modifying the ASIC module to match its clock rate to that of the system processor.

VII. Former opponent 02 had withdrawn its opposition during the opposition proceedings (letter dated 21 January 2004).

VIII. The appellant (opponent) requested that the decision under appeal be set aside and that the patent be revoked.

IX. The respondent (patentee) requested that the appeal be dismissed (main request), or that the patent be maintained in amended form on the basis of one of the auxiliary requests 1 or 2 filed with letter dated 10 July 2006.

Reasons for the Decision

1. The appeal is admissible.

2. The novelty of claim 1 of the main request is not in dispute.

Scope of Claim 1 according to the main request

3. The electronic postage meter control system according to claim 1 of the patent as granted comprises at least a programmable microprocessor, program memory means and an integrated circuit which has an address decoding module (20), timer registers and timer means (600). According to the description and the figures of the granted patent, the control system of the invention is for controlling an electronic postage metering system and more particularly a thermal printing postage meter (patent specification, column 1, lines 3 and 4; column 2, lines 39 to 41; column 3, lines 20 to 23). This is not disputed by the appellant.

3.1 According to claim 1, control signals generated by the address decoding module enable writing of timing data generated by program memory means in the timer registers in response to an address placed on a bus by the microprocessor and the timer means are responsive to said timing data for generating timing signals. The structure and functions of the integrated circuit specified in the claim do not necessarily imply that this integrated circuit must be a single application specific integrated circuit (ASIC). This interpretation is consistent with the description of the patent in suit (column 3, lines 34 to 38) which specifies that the ASIC circuit may comprise various integrated circuit modules. Moreover, the skilled person reading claim 1 in the light of the description has no reason to understand that the timing signals generated in the integrated circuit under the control of the microprocessor of the control system are for controlling the timing of this microprocessor (column 2,

lines 2 to 7; column 3, lines 13 to 19; column 3, line 50 to column 4, line 27). The timing data according to claim 1 are necessarily predetermined data to be used when the program is executed by the control system, because they are generated by program memory means.

Closest prior art

4. The Board cannot share the appellant's view according to which document D4 forms the closest prior art and judges that document D1, which relates to an electronic postage meter system, is the closest prior art to be treated as the starting point of the invention.

4.1 D1 discloses an electronic postage meter (figure 3) which comprises printing means (56) for printing postage indicia (details in figure 9), accounting means (58; details in figure 8) having memory (128) for accounting the postage printed by the printing means and a control system for controlling the postage meter system (75; details in figures 4 and 6). The control system shown in figure 6 includes a programmable microprocessor (100), a program memory (102), an integrated circuit (101) and is in bus communication with the accounting means (page 17, line 10 to page 18, line 26). D1 thus relates to the same technical field as the patent in suit. It discloses a control system which is for a similar use as the control system of claim 1 and comprises the features recited in the preamble of claim 1. Accordingly, D1 is considered as the starting point for assessing the inventive merits of the invention.

4.2 D4 relates to a control unit (100) for controlling a microcomputer, which may be intended for desktop applications and includes, *inter alia*, a microprocessor, "interfaces to video, keyboard, floppy disks, serial and parallel ports, scsi devices, and a mouse pointing device" (for instance, column 1, lines 50 to 57). This control unit comprises a system controller (50) which is an application specific integrated circuit (ASIC) (column 6, lines 42 and 43). According to D4, the system controller provides control, timing and clock signals which are used for synchronising all the subsystems of the microcomputer, including the control, timing and clock frequency of the microprocessor (column 3, lines 16 to 20; column 6, lines 18 to 25 and lines 50 to 52; column 13, lines 28 to 60), based on information received from these subsystems (column 5, lines 64 to column 6, line 17; claim 1). The purpose of the system controller of D4 is to allow a microcomputer, which would accept faster processor and memory technologies, and still incorporate bus technology, to operate with slower peripheral and accessory devices (column 2, lines 17 to 23).

4.3 Accordingly, D4 does not relate to a control system for a use similar to that of the patent in suit in a closely related technical field. It should be noted that the control unit (100) in D4 does not have a microprocessor. The structure and the purpose of the control unit of D4 thus differ substantially from that of the claimed control system. Accordingly, there is no good reason to consider the control unit for a general purpose microcomputer disclosed in D4 as the starting point for the claimed postage meter control system.

Inventive step - Claim 1 of the main request

5. The program memory means (102) disclosed in D1 stores a program for the control system which comprises the steps and functions necessary for formatting and transferring signals for communication with the other postage meter units (page 17, lines 17 to 19; page 18, lines 20 to 26). The integrated circuit (101) is a timer circuit for enabling serial and asynchronous communication to and from the accounting means (pages 17 and 18, bridging sentence; pages 24 and 25, bridging paragraph; page 26, lines 23 to 27). However, D1 does not disclose an integrated circuit having an address decoding module, timer registers and timer means for generating timing signals in response to timing data generated by program memory means, according to the characterizing part of claim 1.

6. Starting from D1 and having regard to the effects provided by the claimed invention, the objective technical problem addressed by the invention could be seen as enabling an electronic postage meter control system to work with microprocessors having a different operating frequency. The solution consists in providing the control system with an integrated circuit which generates programmable timing signals matching the operating clock rate of circuits of the control system to that of the microprocessor chosen (see published patent specification, column 2, lines 2 to 7).

7. In the judgement of the Board, the appellant has not proved that the subject-matter of claim 1 of the main request does not involve an inventive step having

regard to the teachings of the prior art documents on file, and particularly D1 and D4.

7.1 In D1, the communication between the three units of the postage meter is effected in an asynchronous mode. This is achieved by providing each of these units with a crystal controlled clock, by assuring that if a signal is present, it must be present within a given time period and by checking that communication signals are correctly received by returning the signals to the transmitter for comparison (pages 24 and 25, bridging paragraph). Starting from D1, the skilled person faced with the objective technical problem of the invention would thus find in the relevant general common knowledge no obvious reason for operating the control system in a synchronous mode and for deriving timing signals from timing data stored in the program memory means of the control system of figure 6 which contains the program steps (but no timing data) necessary for its operation (page 26, lines 23 to 27).

7.2 The problem addressed in D4, i.e. controlling the flow of data between microprocessors and other elements of the system operating at different nominal speeds, may be regarded, at a certain level of generality, as being similar to the objective problem addressed by the invention when starting from D1. It may also be true that the control unit disclosed in D4 comprises logic circuits responsive to the speed of the microprocessor (figure 2; PAL 52,53), timer registers and timer means for generating timing and clock signals. However, as explained above, D4 does not relate to a control system for a use similar to that of the patent in suit in a closely related technical field. The complex structure

of the apparatus described in D4, the control unit of which, as noted above (paragraphs 4.2 and 4.3) includes an application specific integrated circuit, but no microprocessor, differs substantially from that of the control system and postage meter described in D1. The appellant has not identified any address decoding modules in D4 to enable writing of timing data from program memory means. Thus, it cannot be said that the problem of the invention and the problem solved in D4 are identical in the same technical context and that the invention resides only in incorporating the solution of D4 in the control system of D1.

7.3 According to decision T 05/81 (OJ 1982 249, reason 11), "The comparison of the problem indicated in or deriving from a prior document with that indicated in an application, must avoid an excessively abstract approach; as the degree of abstraction increases so does the likelihood of discovering points of similarity, but at the same time the approach becomes further removed from the thinking of the person skilled in the art... Therefore, the teaching of a document may have narrower implications for a person skilled in the art and broader implications for the potential inventor who first recognises the problem on which the future invention is to be based. The assessment of inventive step must consider solely the limited teaching for the person skilled in the art". The Board judges that these considerations apply in the present case to the comparison of the problem indicated in D4 with the objective problem addressed by the invention and consequently that the skilled person would not have considered the combination the teachings of D1 and D4. Furthermore, such a combination would not lead to the

claimed invention without making modifications to the teaching of these documents which could only be contemplated with the benefit of hindsight.

8. For the foregoing reasons, in the Board's judgement the subject-matter of the claims of the patent in suit (i.e. the claims according to the main request) is considered to involve an inventive step within the meaning Article 56 EPC. The grounds for opposition mentioned in Article 100 EPC thus do not prejudice the maintenance of the patent in suit unamended (Article 102(2) EPC).

Order

For these reasons it is decided that :

The appeal is dismissed.

The Registrar: The Chairman:

U. Bultmann W.J.L. Wheeler