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Datasheet for the decision of 16 March 2007

Case Number: T 0686/04 - 3.5.01

Application Number: 94119503.4

Publication Number: 0657817

IPC: G06F 12/06

Language of the proceedings: EN

Title of invention:
Control system for an electronic postage meter having a programmable application specific integrated circuit

Patentee:
Pitney Bowes Inc.

Opponent:
Francotyp-Postalia Aktiengesellschaft & Co. KG

Headword:
Programmable ASIC/PITNEY BOWES

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - main and first auxiliary request (no)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0686/04 - 3.5.01

D E C I S I O N
of the Technical Board of Appeal 3.5.01
of 16 March 2007

Appellant: (Patent proprietor)
Pitney Bowes Inc.
World Headquaters
One Elmcroft Road
Stamford, CT 06926-0700 (US)

Representative:
Avery, Stephen John et al.
Hoffmann Eitle,
Patent- und Rechtsanwälte
Arabellastraße 4
D-81925 München (DE)

Respondent: (Opponent)
Francotyp-Postalia Aktiengesellschaft & Co. KG
Triftweg 21-26
D-16547 Birkenwerder (DE)

Representative:
Thoenes, Dieter
Patentanwälte
Schaumburg, Thoenes, Thurn, Landskorn
Postfach 86 07 48
D-81634 München (DE)

Decision under appeal:
Decision of the Opposition Division of the European Patent Office posted 18 May 2004 revoking European Patent No. 0657817 pursuant to Article 102(1) EPC.

Composition of the Board:

Chairman: S. Steinbrener
Members: W. Chandler
G. Weiss

Summary of Facts and Submissions

I. This appeal is against the decision of the opposition division to revoke European patent No. 0 657 817.

II. The opposition division found that claim 1 did not involve an inventive step over the following documents:

D1: EP-A-0 359 235

D3: Philips Semiconductors Data Handbook, "80C51-Based 8-Bit Microcontrollers", March 1993, pages 23 to 30

III. In reply to the proprietor's appeal, the respondent (opponent) filed DE-A-42 29 162 (D4) as evidence that programmable ASICs were known.

IV. In the communication accompanying the summons to oral proceedings, requested by both parties on an auxiliary basis, the Board summarised the issues to be discussed. In reply, the proprietor (appellant) filed a first auxiliary request.

V. At the oral proceedings, the appellant requested that the decision under appeal be set aside and that the patent be maintained as granted, or alternatively on the basis of claims 1 to 7 of the auxiliary request, filed with the letter dated 18 January 2007. The respondent requested that the appeal be dismissed. At the end of the oral proceedings, the Chairman announced the decision.

VI. Claim 1 of the main request (claim 1 as granted with the opposition division’s numeration of the features) reads as follows:

"A control system for generating control signals to control electrical components of an electronic postage meter having:
a) a programmable microprocessor (13) in bus communication with a plurality of memory units (MU), and an integrated circuit (15), ASIC (15), having an address decoding module (20), clock module (1100) for generating a system clock signal, a timer module (600) for generating a timer signal and a plurality of control modules (400,700,1300) for generating respective component control signals;
b) said address decoding module (20) having means for generating a unique combination of memory control signals in response to a respective address placed on said bus by said microprocessor (13);
c) said memory units being enabled for reading and writing of data from and to said memory units in response to respective ones of said memory control signals from said address decoding module (20);
d) said integrated circuit having a plurality of registers (8) for receiving data generated by said microprocessor (13) in response to respective ones of said memory control signals; and
e) said control modules being enabled in response to an address instruction from said microprocessor to read said data from selected ones of said registers (8) such that each control module generates component control signals in accordance with said data."

In claim 1 of the auxiliary request, the last feature is replaced by (with the Board's numeration):

"e1) said control modules being enabled by the address decoding module in response to respective address instructions from said microprocessor; and
e2) when enabled said control modules being operable to read said data from selected ones of said registers (8) such that each control module generates component control signals in accordance with said data."

VII. The appellant argued as follows:

The invention reduced the cost of postage meters by providing an ASIC that was configurable on power-up so that it could be used in different meters.

The problem was how to design a flexible control system suitable for controlling a variety of postage meters. The solution was to use an ASIC with multiple modules, the modules being configurable with parameters. The opposition division's formulation of the problem wrongly contained an element of this solution, namely re-configuring the ASIC.

Claim 1 specified the parameterised control module. In particular, it was important that the address decoding module 20 produced control signals that affected the memory, the registers 8 and the control modules. If there was any doubt about this, claim 1 of the auxiliary request clarified that the control modules were enabled by the address decoding module in response to respective address instructions from the microprocessor.

D1 related neither to postage meters nor ASICs. In D1, data was stored in register group 212 that prevented

the microprocessor from addressing certain memory areas. The memory controller 211 used this data to produce a chip select signal CSI only when the microprocessor accessed a valid memory area. However, the chip select signals CSI did not control the registers 212. The passage at column 7, lines 19 to 26 did not disclose how the data got into the register group 212, but it was not using the memory controller 211. D1 therefore did not disclose feature d) of claim 1.

Another difference was feature e).

D3 used a parameterising technique for programming the counter/timers via registers. There was no suggestion of storing data in the registers using an address decoder. Furthermore, D3 did not disclose the control modules, which were claimed in addition to the timer and clock modules. The combination of D1 and D3 would have led to a configurable timer module, but not to a configurable control module according to features d) and e) of claim 1.

D4 disclosed an ASIC that stored configuration data. It did not disclose or suggest features d) and e) of claim 1. The combination of D1 and D4 came no further than that of D1 and D3.

Thus, none of the prior art disclosed the special technique of using the address decoding module to store parameters in configuration registers and to enable control modules.

VIII. The respondent argued as follows:

Claim 1 only differed from D1 in the use of an ASIC and the details of how the data got into the register group 212.
There was no inventive step in using an ASIC because it was known from D4, which disclosed a programmable ASIC 3 to provide a more flexible circuit (column 1, lines 24 to 27). The ASIC was connected to a bus 5 and had logic 20 with registers for storing parameters (column 3, lines 21 to 30).
There was no inventive step in using an address decoder because in D1, some component, e.g. the memory controller, must have given a signal to allow the data to be stored in the register group 212.

Reasons for the Decision

1. As stated by the appellant, the patent concerns the problem of designing a flexible control system for controlling a variety of postage meters. This is solved by providing a control system with a programmable microprocessor having an application specific integrated circuit (ASIC) that is configurable on power-up so that it can be used in different meters (Figure 1). The ASIC 15 has registers 8 (Figure 2) that can be programmed with the operating parameters for each different type of machine. The parameters that can be programmed include the clock frequency (1100 and paragraphs 10 and 23 and claim 3), the timer (600 and claim 4) and various other "control modules", including the timing for the non-volatile memory (400,

paragraph 21, Figure 4 and claim 6), and the print head controller (1300).

2. It is true that D1 does not relate to postage meters. However, the Board considers that it is an admissible starting document for inventive step. Firstly, because claim 1 is directed to a "control system *for* generating control signals to control electrical components of an electronic postage meter …" (Board's emphasis), the control system being thus only suitable for this purpose. Secondly, D1 relates to a computer system that maintains compatibility with different hardware (see column 1, lines 22 to 31), in particular by using a programmable memory address space (see column 2, lines 2 to 12), which is the general objective and one of the specific objectives of the control system of the patent (see paragraph [0005], and paragraph [0016] and claim 5 of the patent, respectively).

3. It is common ground that, as stated at point 4 of the decision under appeal, D1 discloses a computer system that generates control signals with a programmable microprocessor (Figure 2, 11), memory units (17, 20, 40), an integrated circuit (21) having an address decoding module (211). D1 also discloses that the address decoding module (211) has means to enable the memory units to read and write data, according to features b) and c) of claim 1. Finally, D1 discloses a plurality of registers (212) for receiving data, according to the first part of feature d). Furthermore, the Board agrees and it was not contested by the appellant that it is implicit that the system of D1 must contain a clock module and a timer module and

various additional control modules, such as the bus controller 22.

4. During the proceedings, there was some discussion of whether claim 1 of the main request implied that the registers receive data and the control modules are enabled in response to the same memory control signals as previously specified in the claim. Claim 1 of the auxiliary request clarifies this and the Board prefers to deal with this more limited claim first.

5. The Board agrees with the appellant that D1 does not explain how the data gets into the register group 212, so that it does not disclose that the registers receive data specifically in response to the memory control signals, previously identified as the chip select signals CSI. Similarly, D1 does not disclose that any additional control modules are enabled by the address decoding module (feature e1), to read data from the registers (feature e2).

6. The subject-matter of claim 1 of the first auxiliary request therefore differs from D1 in that:

The integrated circuit is an ASIC.
The registers receive data generated by the microprocessor in response to the memory control signals from the address decoder (second part of feature d).
The control modules are enabled by the address decoding module in response to address instructions from the microprocessor (feature e1) and "read" data from the registers (feature e2).

7. Since one difference is the use of an ASIC, it appears that the appellant is correct in stating that the opposition division's formulation of the problem wrongly contains the element of re-configuring an ASIC. The Board considers that the problem solved is simply to increase the flexibility of the circuit.

8. Apart from being a general aspect of routine design in this field, D1 mentions this problem and provides one solution in the form of a programmable memory address space, as pointed out above. Thus, the Board judges that it is obvious to look for further improvements.

9. The Board agrees with the opposition division and respondent that there is no inventive step in using an ASIC to increase the flexibility of the circuit. Furthermore, as stated at point 5 of the decision, the use of registers for providing flexible configuration of control modules in a microprocessor based circuit is a well known measure. Examples are shown in D3 for the timer/counters in a microcontroller and D4 for an output circuit that can be connected to a central unit via a bus (column 2, lines 10 to 13). D4 even mentions at column 1, lines 24 to 32 that a parameterisable ASIC increases the flexibility of such a control module, i.e. solves the above-mentioned problem. The Board therefore considers that the skilled person would regard using a programmable ASIC in the circuit of D1 to configure any of the control modules as an obvious possibility.

10. In the Board's view, the use of a programmable ASIC in the system of D1 immediately implies the need for the remaining distinguishing features. Firstly, in order to program the ASIC, the registers must receive data from

the microprocessor. It is a matter of routine design to access a module in a computer system via an address decoder and it would have been an obvious design possibility especially in an integrated system to extend the existing address decoder for this purpose according to feature d). Furthermore, it is self-evident that the configuration data for the control module must somehow be transmitted to the control module. Arranging the control modules to "read" this data is an obvious design choice.

11. Accordingly, the subject-matter of the first auxiliary request, and the broader main request, does not involve an inventive step (Article 56 EPC).

12. There being no further requests, it follows that the appeal must be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

T. Buschek S. Steinbrener