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D E C I S I O N
of 14 July 2006

Case Number: T 0681/04 - 3.4.03

Application Number: 95105640.7

Publication Number: 0685878

IPC: H01L 21/48

Language of the proceedings: EN

Title of invention:
Semiconductor package and method of forming the same

Applicant:
FUJITSU LIMITED

Opponent:
-

Headword:
Through hole/FUJITSU

Relevant legal provisions:
EPC Art. 54, 56, 123(2)

Keyword:
"Novelty (yes) - after amendment"
"Inventive step (yes) - after amendment"

Decisions cited:
-

Catchword:
-

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Case Number: T 0681/04 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 14 July 2006

Appellant: FUJITSU LIMITED
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 10 December 2003 refusing European application No. 95105640.7 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. G. O'Connell
Members: G. Eliasson
T. Bokor

Summary of Facts and Submissions

I. This appeal is against the refusal of European patent application No. 95 105 640.7 for the reason that the subject matter of claim 1 was not new having regard to the prior art document

D6: WO 91 11 025 A.

II. In the examination procedure, the following documents among others were cited:

D1: IBM Technical disclosure Bulletin, vol. 32, No. 8a, January 1990, pages 178 to 179; and

D3: IEEE Transactions on Components, Hybrids, and Manufacturing Technology, vol. 15, No. 1, February 1992, pages 103 to 106.

III. In response to a communication from the board, the appellant proprietor filed amended application documents with the letters dated 10 July 2006 and 11 July 2006.

IV. The appellant applicant requests that the decision under appeal be set aside and that a patent be granted on the basis of the following documents:

Claim 1 filed with the letter dated 11 July 2006

Description:

pages 2 and 6 to 25 as originally filed
pages 1, 1a filed with letter dated
1 February 1999

page 3 filed with letter dated 29 August 2000
page 3a filed with letter dated 10 July 2006
(pages 4 and 5 deleted without replacement)

Drawings sheets 1/19 to 19/19 as originally filed.

V. Claim 1 according to the appellant applicant's request reads as follows:

"1. A semiconductor device comprising:

a printed circuit board (31) having through-holes (22A), including an inner layer (24A-2) made of copper and filled with a filling core (52) of a synthetic resin,

an additive layer (51) provided on an upper surface of said printed circuit board (31) as well as an upper surface of said filling core (52) providing support for said additive layer (51),

said additive layer (51) including an insulator layer (56) and a wiring pattern provided on the insulator layer (56), said wiring pattern having one or more paths electrically connected with said inner layer, and said filling core being in direct contact with a portion of the insulator layer (56) that is situated over the filling core;

a semiconductor chip (32) fixed on an upper surface of said additive layer (51) and having solder balls (40) electrically connected with said one or more paths; and

nodes (13A) provided on a lower surface of said printed circuit board (31), said nodes being electrically connected with said solder balls via said inner layer and said one or more paths,

characterized in that

said support allows said one or more paths to be laid out without a passage restriction imposed by said through-holes (22A) and said one or more paths include at least one path which traverses at least one upper surface of said through-holes ($22A_1$ to $22A_5$)."

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments*

Claim 1 contains the features of claims 1 and 2 as filed with the additional specification that (i) the board (31) is a printed circuit board; the inner layer (24A-2) is made of copper; (iii) the filling core is made of a synthetic resin; (iv) the additive layer includes an insulator layer (56) and a wiring pattern on the insulator layer, where the filling core is in direct contact with a portion of the insulating layer that is situated over the filling core; and (v) the semiconductor chip (32) has solder balls (40). These features are disclosed in the application as published on column 6, lines 31 to 35, column 7, line 54 to column 8, line 7, column 6, lines 2 to 23, respectively.

3. *Novelty*

3.1 In the decision under appeal, document D6 was considered novelty-destroying prior art. It discloses a semiconductor device comprising a printed circuit board 20 (Figure 3) having through holes 56 which are filled with a filling core 52 of metal (Figures 3 to 5; page 9, line 25 to page 10, line 11). An additive layer 21 - 26 is provided on the printed circuit board and comprises an insulating layer 22 and a wiring layer 24 on the insulating layer (Figure 3; page 8, lines 11 to 25). A semiconductor chip is to be fixed on the upper surface of the additive layer and has solder balls electrically connected with one or more electrical paths (page 10, lines 2 to 8). Nodes 53a-d are provided on a lower surface of the circuit board 20 which are electrically connected to the solder balls of the semiconductor chip via the through holes. As the through-hole structure is flat, the upper electrical paths in the additional layer are laid out without a passage restriction imposed by the through holes, and as shown in Figure 4, at least one path traverses one of the through holes.

3.2 The subject matter of claim 1 differs from the device of document D6 in that the through holes have each an inner layer made of copper and are filled with a synthetic resin, whereas in document D6, the through holes are filled with metal. Furthermore, the filling core made of a synthetic resin is in direct contact with a portion of the insulator layer of the additive layer formed over the filling core. In the device of

document D6, a conductive wiring layer is in direct contact with the filling core.

3.3 In claim 1 which formed the basis for the decision under appeal, the printed circuit board was termed "board base" which enabled the examining division to equate the "board base" with the first insulating layer 22 formed between the wiring layers. Claim 1 as amended, however, no longer lends itself to such an interpretation.

Hence the subject matter of claim 1 is new with respect to document D6.

3.4 Document D1 discloses a semiconductor device comprising a printed circuit board having a through hole with a conductive inner layer for establishing an electrical connection between a semiconductor chip fixed to the upper surface of an additive layer formed on the printed circuit board and nodes provided on a lower surface of the circuit board (Figure). As argued by the applicant in the examination procedure, document D1 does not disclose whether the through holes are filled at all. In any case, the contact structure to the through hole in the device of document D1 is formed directly over the through hole, which has as a consequence that if the through hole were filled with filling core of an insulating material, the insulator layer of the additional layer would not be in contact with the filling core as specified in claim 1.

3.5 Document D3 discloses a semiconductor device comprising a printed circuit board ("aromatic-epoxy lamination") with an additional layer formed on the printed circuit

board and comprising a lamination of an insulating layer ("First level") and wiring patterns (see Figure 1). A through-hole ("Copper through-hole") is formed through the different insulating layers within the additional layer. A semiconductor chip having solder bumps is fixed on the upper surface of the additional layer where the solder bumps are electrically connected with the paths of the wiring pattern.

The device of claim 1 differs from that of document D3 in that the through-holes have an inner layer made of copper and are filled with a filling core of a synthetic resin. Document D3 does not disclose any details as to the construction of the through-holes. Furthermore, however, Figure 1 of document D3 does not discloses any paths of the wiring pattern traversing an upper surface of a through-hole.

3.6 For the above reasons, the subject matter of claim 1 is new within the meaning of Article 54 EPC.

4. *Inventive step*

4.1 Document D6 is considered to be the closest prior art. As discussed above, the claimed device differs from that of document D6 in that it has at least one through-hole which has an inner layer made of copper and is filled with a synthetic resin, whereas in document D6, the through-holes are completely filled with metal. Although document D1 discloses a through-hole with a conductive inner layer, a skilled person applying the teaching of document D1 to the device of document D6 would then use the upper contact to the

through-hole as disclosed in document D1. As discussed under item 3.4 above, this contact structure prevents the insulator layer of the additive layer from being in direct contact with a portion of the filling core of the through hole, which is the case for the claimed device. Moreover, in contrast to the claimed device, the contact structure of document D1 prevents the paths of the wiring path from traversing the upper surfaces of the through-holes, and therefore, the wiring path cannot be laid out without a passage restriction imposed by the through hole.

4.2 For the above reasons, in the board's judgement, the subject matter of claim 1 involves an inventive step within the meaning of Article 56 EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent with the following documents:

   Claim 1 filed with the letter dated 11 July 2006

   Description:

   pages 2 and 6 to 25 as originally filed
   pages 1, 1a filed with letter dated 1 February 1999
   page 3 filed with letter dated 29 August 2000
   page 3a filed with letter dated 10 July 2006
   (pages 4 and 5 deleted without replacement)

   Drawings sheets 1/19 to 19/19 as originally filed.

Registrar	Chair
S. Sánchez Chiquero	R. G. O'Connell