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D E C I S I O N
of 17 November 2005

Case Number: T 0668/04 - 3.5.03

Application Number: 88114341.6

Publication Number: 309763

IPC: H04J 3/07

Language of the proceedings: EN

Title of invention:
Multiplexer and demultiplexer apparatus adaptable for two kinds of transmission rates

Patentee:
NEC CORPORATION

Opponent:
Siemens AG

Headword:
-

Relevant legal provisions:
EPC Art. 52(1), 56
RPBA Art. 10b

Keyword:
"Inventive step (no) - all requests"

Decisions cited:
-

Catchword:
-

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Case Number: T 0668/04 - 3.5.03

D E C I S I O N
of the Technical Board of Appeal 3.5.03
of 17 November 2005

Appellant: (Proprietor of the patent)
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Decision under appeal: **Decision of the Opposition Division of the European Patent Office posted 24 March 2004 revoking European patent No. 309763 pursuant to Article 102(1) EPC.**

Composition of the Board:

Chairman: A. S. Clelland
Members: D. H. Rees
M.-B. Tardo-Dino

Summary of Facts and Submissions

I. This is an appeal by the proprietor of European Patent No. 0 309 763 against the decision of the opposition division to revoke the patent.

II. The independent claims as granted read as follows:

"1. A multiplexer apparatus for multiplexing four low-speed bit streams into a single high-speed bit stream, comprising:
buffer memory means (5), of which one unit is provided for each of the four low-speed bit streams, for temporarily storing the four low-speed bit streams;
reference clock pulse generating means (1) for generating a reference clock pulse (f_0) for the operation of the multiplexer apparatus; and multiplexer means (10) responsive to the read clock pulse for multiplexing the four low-speed bit streams read out of the buffer memory means into the high-speed bit stream;
characterized by
pulse generating means (2) for frequency-dividing the reference clock pulse (f_0) by a predetermined number and generating read and write clock pulses for the buffer memory means (5), wherein the frequency dividing ratio is altered according to a selection signal (4), so that the pulse generating means (2) varies the bit rates of the read and write clock pulses in response to the bit rates of the low-speed bit streams.

4. A demultiplexer apparatus for demultiplexing an inputted single high-speed bit stream into four low-speed bit streams comprising:

reference clock pulse generating means (41) for generating a reference clock pulse (f_0) for the operation of the demultiplexer apparatus;
demultiplexer means (44) responsive to the reference clock pulse for demultiplexing the high-speed bit stream into the four low-speed bit streams;
buffer memory means (45), of which one unit is provided for each of the four low-speed bit streams, for temporarily storing the four low-speed bit streams;
characterized by
pulse generating means (42) for frequency-dividing the reference clock pulse (f_0) by a predetermined number and generating read and write clock pulses for said buffer memory means (5), wherein the frequency dividing ratio is altered according to a selection signal (4), so that the pulse generating means (42) varies the bit rates of the read and write clock pulses in response to the bit rate of the high-speed bit stream."

III. The opponent (respondent) had requested revocation of the patent in its entirety on the grounds that the claimed subject-matter lacked novelty and did not involve an inventive step, citing documents:

D1: W. Paetsch et al., "ELMUX 1000, ein neues ARQ-Multiplexsystem für Funkfernschreiben," Siemens-Zeitschrift 3/71, pages 123 to 129, and

D2: EP 0 099 101 A.

In response to auxiliary requests submitted by the proprietor, the opponent later further cited documents:

D3: F. Bekert et al., "Digitalsignal-Multiplexgeräte DSMX 2/8, DSMX 8/34 und DSMX 34/139," telcom report 2 (1979), Beiheft "Digital-Übertragungstechnik", pages 59 to 64, and

D4: US 4 196 315 A

IV. In oral proceedings held on 10 March 2004, the opposition division found that the subject-matter of granted claims 1 and 4 did not involve an inventive step having regard to document D1 or to a combination of documents D3 and D2. A first auxiliary request was found not to satisfy Article 123(2) EPC and the independent claims of a second auxiliary request (corresponding to Auxiliary Request 3 of the present appeal - see below) did not involve an inventive step having regard to D1. The patent was accordingly revoked, the written decision being dispatched on 24 March 2004.

V. Notice of appeal was filed, with the appropriate fee, with a letter dated 17 and received 18 May 2004. A statement of grounds of appeal was submitted on 2 August 2004.

VI. In the course of the appeal the appellant submitted a number of amended claims as the basis of auxiliary requests. By the end of the oral proceedings, there remained a main request for maintenance of the patent as granted and auxiliary requests 1, 2, 2A, 3 and 3A.

In addition to the features specified in the independent claims as granted, the independent claims of Auxiliary Request 1 specified that the (de)multiplexer apparatus was "adaptable for operation

at two different transmission rates" and that the high-speed bit stream was "at a selected one of two predetermined bit rates".

In addition to the features specified in the independent claims as granted, the independent claims of Auxiliary Request 2 specified that the (de)multiplexer apparatus was "adaptable for operation as a second order MUX [respectively DMUX] apparatus or a third order MUX [DMUX] apparatus".

In Auxiliary Request 2A, the independent claims of Auxiliary Request 2 were further amended to specify that the second order and third order apparatuses conformed to Recommendations G.742 and G.751 respectively.

In Auxiliary Request 3 the independent claims corresponded to granted dependent claims 3 and 6 (as dependent on claims 1 and 4 respectively), i.e. they added to the granted independent claims the feature that "the capacity of the buffer memory means (5) is varied in response to the selection signal (4)."

In Auxiliary Request 3A this same feature was added to the independent claims according to Auxiliary Request 2A. The independent claims of Auxiliary Request 3A read as follows:

"1. A multiplexer apparatus adaptable for operation as a second order MUX apparatus conforming to Recommendation G.742 or a third order MUX apparatus conforming to Recommendation G.751, and for

multiplexing four low-speed bit streams into a single high-speed bit stream, comprising:
buffer memory means (5), of which one unit is provided for each of the four low-speed bit streams, for temporarily storing the four low-speed bit streams;
reference clock pulse generating means (1) for generating a reference clock pulse (f_0) for the operation of the multiplexer apparatus; and multiplexer means (10) responsive to the reference clock pulse for multiplexing the four low-speed bit streams read out of the buffer memory means into the high-speed bit stream;
characterized by
pulse generating means (2) for frequency-dividing the reference clock pulse (f_0) by a predetermined number and generating read and write clock pulses for the buffer memory means (5), wherein the frequency dividing ratio is altered according to a selection signal (4), so that the pulse generating means (2) varies the bit rates of the read and write clock pulses in response to the bit rates of the low-speed bit streams, wherein the capacity of the buffer memory means (5) is varied in response to the selection signal (4).

3. A demultiplexer apparatus adaptable for operation as a second order DMUX apparatus conforming to Recommendation G.742 or a third order DMUX apparatus conforming to Recommendation G.751, for demultiplexing an inputted single high-speed bit stream into four low-speed bit streams comprising:
reference clock pulse generating means (41) for generating a reference clock pulse (f_0) for the operation of the demultiplexer apparatus;

demultiplexer means (44) responsive to the reference clock pulse for demultiplexing the high-speed bit stream into the low-speed bit streams;
buffer memory means (45), of which one unit is provided for each of the four low-speed bit streams, for temporarily storing the four low-speed bit streams;
characterized by
pulse generating means (42) for frequency-dividing the reference clock pulse (f_0) by a predetermined number and generating read and write clock pulses for said buffer memory means (5), wherein the frequency dividing ratio is altered according to a selection signal (4), so that the pulse generating means (42) varies the bit rates of the read and write clock pulses in response to the bit rate of the high-speed bit stream, wherein the capacity of the buffer memory means (5) is varied in response to the selection signal (4)."

VII. The appellant requested that the decision under appeal be set aside and that the patent be maintained, as granted or alternatively on the basis of claims 1 and 4 of Auxiliary Request 1 filed with the letter of 27 October 2005, or claims 1 and 4 of Auxiliary Request 2 or 2A filed during the oral proceedings or claims 1 to 4 of Auxiliary Request 3 filed with the grounds of appeal, or claims 1 to 4 of Auxiliary Request 3A as filed during the oral proceedings.

The respondent requested that the appeal be dismissed.

VIII. The decision of the board was announced at the end of the oral proceedings.

Reasons for the Decision

1. As to the admissibility of the auxiliary requests, all the amendments filed by the appellant were in response to arguments put forward by the respondent or the board and had been foreshadowed in the discussion of those arguments. The respondent further explicitly agreed to the admission of the new requests filed during the oral proceedings. The board therefore exercised its discretion pursuant to Article 10b RPBA to admit all the appellant's auxiliary requests.

2. The board heard the parties' arguments and considered the appellant's requests in their order of priority at the oral proceedings. The board came to the conclusion in every case that the subject-matter of the independent claims did not involve an inventive step. Since the independent claims of Auxiliary Request 3A include all the features specified in the respective independent claims of each of the other requests, and the reasoning with regard to this request is immediately applicable to each of the other requests, it suffices in the written reasons to discuss only this request in detail.

3. The claimed invention relates to multiplexers and the corresponding demultiplexers. The arguments relating to the multiplexers apply equally *mutatis mutandis* to the demultiplexers, a point disputed by neither party. Therefore for the sake of clarity the following reasoning will concentrate on multiplexers and the subject-matter of claim 1.

4. A number of years before the priority date of the contested patent, the CCITT organisation issued a number of recommendations relating to a hierarchical arrangement for transmission of telephone calls. At the lowest level 30 telephone calls, each converted into binary signal form at 64 kbps, are transmitted using time sharing on a single line which has a data rate of 2048 kbps (circa 2 Mbps). At the next stage, four of these lines are concentrated into one line with a data rate of 8 Mbps, at the next four 8Mbps lines are concentrated into one 34 Mbps line, and at the next four 34 Mbps lines are combined into one 139 Mbps line. At each stage a format for the signals is defined, specifying a "frame" consisting not only of a certain number of data bits, but also of other signals, including bit patterns indicating the start of a frame and "stuff bits" (which will be discussed later). The recommendations relating to the 2M/8M multiplexer and the 8M/34M multiplexer are G.742 and G.751 respectively. The patent in suit and D3 give relevant details of these recommendations, including the respective frame formats (patent column 1, "Background of the Invention" and Fig. 1, and D3 page 60, Bild 2). According to the patentee, the inventor noted the similarity of these frame formats and had the idea, in itself not obvious, to design a multiplexer which could be used either for 2M/8M multiplexing or 8M/34M multiplexing. This led to increased efficiency in design, lower unit costs and more flexibility for the end user. Since the principal difference in the frame formats is the number of bits per frame, the inventor provided a counter for frequency division of the basic clock with a settable divider to provide a frame pulse every 848 or 1536 clock pulses. Thus this counter could be employed in a

multiplexer which could be used for G.742 multiplexing or for G.751 multiplexing.

5. The patent describes, and independent claim 1 according to Auxiliary Request 3A claims, a further adaptation in the multiplexer, namely a buffer having a variable capacity. The transmission system according to the recommendations of CCITT is a "plesiochronous" one, which means that the clock rates of sender and receiver are known and are nominally the same, but they may vary within certain small limits. It would have been known to the skilled person and is mentioned without being discussed in detail in the patent (see column 4, lines 4 to 13), that in order to accommodate differences, each multiplexer stage inserts a variable number of "stuff bits" into its frames. It would have been clear to the skilled person that in order to determine how many stuff bits to insert into each frame and to carry out the insertion, a first-in-first-out (FIFO) buffer of some length would be necessary. The patent also mentions "jitter" (short-term variation in timing) as a reason for the buffer - see column 7, lines 7 to 9.

6. The patent gives no specific reason why the required buffer length for G.742 (m) should be different to that required for G.751 (n), and indeed contemplates all the possibilities of $m < n$, $m = n$ and $m > n$ (column 7, lines 9 to 11).

Rather than seeing the problem as the two recommendations requiring different length FIFO buffers, the appellant suggested that the length was changed in order to free up memory for other purposes. However,

this is merely speculative; there is absolutely no indication of such a purpose in the disputed patent. Moreover the board finds the suggestion rather implausible. All that would be freed up is a very small amount of memory in a specific FIFO configuration; it seems very unlikely that it would be worth the probably extensive extra logic required to make it available for another purpose.

At any rate a buffer with selectable choice of two lengths is supplied, the selection being based on the signal indicating which recommendation the multiplexer is operating to, as also for the counter.

7. The appellant argued that the problem faced by the skilled person with respect to document D3 was, as formulated by the opposition division in its decision, to improve efficiency and reduce costs of the multiplexer system described in that document. The achievement of the invention was to supply a multiplexer apparatus which could be used for either of the recommendations G.742 or G.751, no such apparatus being disclosed in the prior art put forward by the respondent. Indeed the patent also states this as the advantage resulting from the invention - see column 7, lines 33 to 41. However, as pointed out by the respondent, the only embodiment given in the description of the contested patent does not disclose such a multiplexer apparatus. It was pointed out, and could not be disputed by the appellant, that according to the structures shown (e.g. Fig. 3, together with column 3, lines 21 to 24), the G.742 and G.751 multiplexers would need different reference clock generators (element 1 in Fig. 3). There is no

indication in the patent that a reference clock generator with a selectable frequency is contemplated. The respondent also alleged that in practice other parts of the apparatus would need to be adapted for operation according to the two recommendations; however, no evidence was advanced on this point. At any rate it is clear that the features claimed, and described, do not by themselves achieve the advantage as presented by the appellant, namely a common apparatus for the two recommendations. Thus the board cannot take this problem into account when assessing the question of an inventive step. What is disclosed and claimed is a multiplexer apparatus which can be adapted to conform to recommendations G.742 and G.751 by changing certain components, but which also has certain components common to both "models", namely the counter and the buffer. Thus the objective technical problem solved by the claimed invention is how to share at least some components between G.742 and G.751 multiplexers. It is solved by making the behaviour of the counter and the buffer dependent in part on a selection signal.

8. D3 describes a family of products to carry out the multiplexing of the various stages of the CCITT hierarchy. The appellant argued that D3 does not point out any problem to be solved, in particular not the problem of improving efficiency and decreasing cost. However, in the view of the board firstly this problem would always be considered by the skilled person when deciding how to implement systems, and secondly when presented with a requirement for a family of related products, as in D3, it would be a routine measure for the skilled person to consider the extent to which components could and should be shared. The potential

advantages of such sharing would be known to the skilled person, e.g. lower design costs and possibly lower unit manufacturing costs based on the production of larger quantities, as would the possible disadvantages, e.g. having to produce parts able to cope with the speed requirements of a higher hierarchy level, even if they are not actually going to be used at that level.

9. The skilled person, considering the problem of how to share components between members of the product family, would take into account document D2, which teaches that a common counter can be supplied for different multiplexer apparatuses; different frame lengths are dealt with by providing a selection signal (D2, page 7, lines 18 to 26, and page 8, lines 20 to 22). While D2 shows an embodiment having multiplexers with input/output rates 34/140 and 140/565 (page 6, lines 28 to 30), it would be clear to the skilled person knowing the formats of the relevant frames (D3, page 60, Bild 2) that this document's teaching would be equally applicable to the G.742 2/8 and the G.751 8/34 multiplexer apparatuses.

10. Thus with respect to the subject-matter of claim 1, document D3 shows "second order" G.742 and "third order" G.751 multiplexer apparatuses, each for multiplexing four low-speed bit streams into a high-speed bit stream (D3 page 60, column 3, lines 10 to 35). The skilled person would know (see point 5 above) that these apparatuses would require buffer memory means of which one unit is provided for each of the four low-speed bit streams, for temporarily storing the low-speed bit streams, in order to implement the stuff bits

method also disclosed in D3 (in the same passage). It would be further elementary to the person skilled in the art, that such multiplexers in a plesiochronous environment would have their own reference clock pulse generating means from which the read and write clocks would be derived. Thus, with the possible exception of the claim being directed to a multiplexer apparatus "adaptable for operation" according to two different recommendations, all of the features in the pre-characterising part of the claim are either explicitly disclosed in D3 or would have been implicit to the skilled person. The appellant did not contend that any of these features were new or involved an inventive step.

11. With respect to the first characterising feature the subject-matter of claim 1 is not entirely clear; in particular, it is not clear what was intended by the "read and write clock pulses" claimed, since the only pulses clearly "for the buffer memory means" as claimed have frequency f_0 and these are not the result of the selectably variable division carried out by unit 22 in Fig. 3. It is also noted that the selectable-length buffer 5 in Fig. 2 is not shown as having any input from the "F. P. Gen" (i.e. "frame pulse generator") 3. Since however a lack of clarity of the claim, insofar as it does not arise from amendments after grant, is not a ground of opposition, the board concludes that the claimed subject-matter, with regard to this feature, must be interpreted as a generalisation encompassing, possibly among other things, the embodiment described. Since D2 describes precisely the same idea of providing a selectably variable divider for producing frame pulses as is shown in the description of the patent and

there is no other disclosure in the description of the patent to which the claimed feature can be referring, the board also concludes that the feature of claim 1, "pulse generating means ... low-speed bit streams" is shown by D2. Further, for the reasons given above at points 8 and 9, the skilled person would have been motivated to apply the teaching of D2 to the G.742 and G.751 multiplexer apparatuses of D3.

12. Moreover in the light of the teaching in D2 that necessary adaptations in the frame structure can be accommodated by using a selectable counter, the skilled person, faced with a necessity for different length FIFO buffers in implementing apparatuses conforming to the two recommendations, would apply the same principle to provide a FIFO which can be used by both apparatuses by making its length selectable, thus arriving at the last feature of claim 1 without involving an inventive step.

13. Finally, with respect to the question whether the resulting apparatus is "adaptable to operate as a second order MUX apparatus conforming to Recommendation G.742 or a third order MUX apparatus conforming to Recommendation G.751", the board concludes that it is adaptable to the extent that the apparatus disclosed in the patent also is, i.e. by replacing some components not including the selectable frequency dividing ratio pulse generating means and the selectable length buffer memory - see point 7 above.

14. As a counter-indication that the claimed subject-matter is inventive the appellant argued that document D3 was, in the context of a fast-moving technical field,

relatively old, having been published in 1979, compared to the priority dates of the patent in 1987 and 1988. This argument was put forward based on the premise that the patent disclosed a multiplexer apparatus which could be used for either G.742 or G.751 multiplexing stages. It was suggested that if such an apparatus had been obvious it would have been discussed in a publication of some sort in the intervening years. However, the board has concluded that the patent does not actually disclose such a multiplexer - see point 7 above. It rather discloses the sharing of certain components within a family of multiplexers. This idea was disclosed by D2 whose priority date was 13 July 1982, and which was published on 25 January 1984. The board further considers that the question which components should be common to which members of the family of products is a matter related to various commercial and technical factors which may have changed during the period in question (which is approximately three years rather than the eight years suggested by the appellant), so that the absence of a document revealing precisely the features claimed is not a convincing argument for the claimed invention involving an inventive step.

15. Thus the subject-matter of claim 1 of Auxiliary Request 3A does not involve an inventive step and the request is not allowable. Since the same reasons are immediately adaptable to the independent claims of all the other requests, there is no allowable request and the appeal must be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

D. Magliano A. S. Clelland