BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [X] To Chairmen
(D) [ ] No distribution

Datasheet for the decision of 24 July 2007

Case Number: T 0179/04 - 3.5.01

Application Number: 98960426.9

Publication Number: 1034479

IPC: G06F 11/267, G 01R 31/3185, H03K 19/177

Language of the proceedings: EN

Title of invention:
Test circuitry for ASICs

Applicant:
Lightspeed Semiconductor Corporation

Opponent:
-

Headword:
Test circuitry/LIGHTSPEED SEMICONDUCTOR

Relevant legal provisions:
EPC Art. 84

Keyword:
"Support - amended claim (yes)"

Decisions cited:
-

Catchword:
-

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0179/04 - 3.5.01

D E C I S I O N
of the Technical Board of Appeal 3.5.01
of 24 July 2007

Appellant: Lightspeed Semiconductor Corporation
1151 Sonora Court
Sunnyvale, CA 94086 (US)

Representative: Jackson, Robert Patrick
Frank B. Dehn & Co.
St Bride's House
10 Salisbury Square
London EC4Y 8JD (GB)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 22 July 2003 refusing European application No. 98960426.9 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: S. Steinbrener
Members: W. Chandler
G. Weiss

Summary of Facts and Submissions

I. This appeal is against the decision of the examining division to refuse the application because claim 1 of the main request lacked support and essential features (Article 84 EPC). The argument was essentially that the claim only mentioned storing test data values in the bit storage units of the ASIC, but lacked the concept of shifting the data into the bit storage units with a clock signal (reasons for the decision, point 4). The decision states that all the embodiments implement the shifting function by using a control multiplexer and a test clock, and the first auxiliary request containing these features was allowed at the oral proceedings. However, the appellant did not approve the text for grant, but maintained the main request, and the application was refused.

II. In the grounds of appeal, the appellant argued that claim 1 of the main request contained all the essential features of the invention.

III. In the communication accompanying the summons to oral proceedings, the Board stated that it would have to be discussed at the oral proceedings whether the generalisation to a bit storage unit for storing the test data value, without any mention of how the data was put there or retrieved, was warranted in the light of the description. The Board further stated that if the appellant were to make an allowable amendment to specify that storing was performed by shifting test data from other blocks or by daisy-chaining the bit storage units, the Board would probably consider such an amended main request to fulfil the requirements of

Article 84 EPC and remit the case to the department of first instance for further examination.

IV. After several telephone conversations to clear up some discrepancies in amended claim versions, the appellant filed, in a response dated 16 July 2007, an amended main request containing a new claim 1 that was in line with the requirements considered necessary by the Board.

V. The appellant requested that the decision under appeal be set aside and that the application be remitted for grant in the form set out in the communication under Rule 51(4) EPC, dated 11 November 2002, as amended by claims 1 to 18 and description pages 10 and 10a filed with the response of 16 July 2007 (main request), or alternatively in the form of the auxiliary request set out in said communication under Rule 51(4) EPC. In case of a remittal on the basis of the main request, the oral proceedings should be cancelled.

VI. The oral proceedings were cancelled.

VII. Claim 1 of the main request reads as follows:

"An integrated circuit (400), comprising an array (410) of predesigned logic blocks (420) arranged in rows and columns and couplable to form a user-designed circuit, each logic block (420) comprising a data input (DS, DA, SC, SX, S2, MC, EN, AS), a data output (Q), a test data input (TD) and a bit storage unit (670, 688), wherein each logic block (420) is selectable to operate in one of a normal mode of operation to perform a user-designed function as an operative part of said user-designed circuit, whereby data received at the data

input (DS, DA, SC, SX, S2, MC, EN, AS) is processed to generate a result at the data output (Q), and a test mode of operation, whereby the bit storage unit (670, 688) stores a test data value received at the test data input (TD) and the data output (Q) of the logic block outputs the stored test data value,
characterised in that the predesigned circuit comprises a plurality of row mode select lines and a plurality of column mode select lines, and each logic block (420) in a respective row is coupled to a row mode select line associated with said respective row and each logic block (420) in a respective column is coupled to a column mode select line associated with said respective column and each logic block (420) is selectable to operate in said normal mode of operation by signals carried on said row mode select line and said column mode select line while simultaneously other logic blocks (420) in said array (410) of logic blocks (420) operate in said test mode of operation, and in that when in the test mode of operation, the logic blocks (420) are daisy-chained together such that data can be passed from the output (Q, TQ) of a first logic block (420) to the test data input (TD) of a second logic block (420), and the logic blocks (420) are arranged to shift data from the test data input (TD) into the bit storage unit (670, 688) and out in response to a test clock signal."

VIII. The appellant argued essentially as follows:

Any suitable arrangement of components may be used to shift test data into the bit storage units and it was unnecessary to limit the claims to an arrangement comprising a multiplexer and a test clock signal as in

claim 1 of the auxiliary request before the examining division.

Reasons for the Decision

Background

1. The application concerns the problem of testing application specific integrated circuits (ASICs). In "scan" testing (pages 2 to 4 and Figure 1a), the flip-flops already present in the user's circuit design are daisy-chained together and used for testing the circuit. Essentially, the normal operation of the ASIC is stopped and external test data is shifted into the flip-flops. Normal operation of the circuit is resumed for a short time, say a single clock cycle, and then stopped again. The flip-flops now contain new values that represent another state of the circuit. These values are shifted out of the flip-flops and compared with what the values should be, e.g. derived by simulating the circuit. Any differences can be used to determine various faults in the circuit.

2. The invention is an ASIC with an array of a specific type of logic blocks 420/444 (Figures 5 and 6) each having bit storage units 670, 688 (pages 16 to 20). The logic blocks are essentially modified so that in a test mode they are daisy-chained together to behave like the flip-flops in the prior art scan testing techniques (pages 20 to 24 and Figure 11). The bit storage units store the test data that is used to test the circuit and also store the output values of the test. This is said to be advantageous over the prior art because it

does not require prior knowledge of the circuit or involve the designer (page 21), or require additional flip-flops (page 9).

3. Another aspect of the invention, subject of the first feature of the characterising part of claim 1, is that each function block is addressable, allowing arbitrary groups of blocks, in particular non-adjacent blocks, to be tested – "partition test". This is said to be faster than individual testing of each block (pages 25 to 29).

Main request

4. Claim 1 of the main request was refused for not fulfilling the requirements of Article 84 EPC. From the statement setting out the grounds for appeal, it appears that the appellant interpreted the appealed decision in a way that the examining division considered the provision of a multiplexer and a test clock essential for the invention (see page 2 of the statement of grounds, second paragraph).

5. The Board tends to agree with the appellant that it is indeed not necessary to limit the claim to the shifting mechanism of the embodiments. However, according to the Board's understanding of the appealed decision, the examining division did not require this either. At the oral proceedings they allowed the auxiliary request, but in the refusal stated that what was missing from claim 1 of the main request was the common basis of all the embodiments and test procedures in the description, namely the concept of shifting the data into the bit storage units with a clock signal (see point 4). The Board agrees with this point of view.

6. Since the appellant has now added the feature of daisy-chaining the logic blocks together and shifting test data into the bit storage unit and out in response to a test clock signal to the end of claim 1, the Board considers the claim to fulfil the requirements of Article 84 EPC. The Board also considers that the amendments are supported by the original application, in particular at page 23, lines 18 to 21 and page 25, lines 19 to 21 and therefore meet the requirements of Article 123(2) EPC.

7. However, since compatibility of the dependent claims and the patentability of the claims of the main request have not been examined in detail with claim 1 in this form, the Board considers it appropriate to remit the case to the examining division for this to be done.

8. Since the case has been remitted on the basis of the appellant's main request, the auxiliary request need not be considered.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance for further prosecution.

The Registrar: The Chairman:

T. Buschek S. Steinbrener