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Datasheet for the decision of 18 July 2007

Case Number: T 0166/04 - 3.5.01

Application Number: 98308284.3

Publication Number: 0911736

IPC: G06F 12/08

Language of the proceedings: EN

Title of invention:
Low occupancy protocol for managing concurrent transactions with dependencies

Applicant:
Compaq Computer Corporation

Opponent:
-

Headword:
Shared memory system / COMPAQ

Relevant legal provisions:
EPC Art. 56, 84, 96(2), 113(1), 116(1), 123(2)
EPC R. 27(1)(c), 51(3), 67, 71(1)
RPBA Art. 10

Keyword:
"Introduction of prior art documents by summons to oral proceedings - procedural violation (no)"
"Selection of amending features from a set of features consistently described as part of the solution - admissible generalisation (no)"
"Inventive step (no - skilled person's natural approach)"

Decisions cited:
T 0409/91, T 0951/92, T 0802/97, T 0404/03

Catchword:
-

Case Number: T 0166/04 - 3.5.01

D E C I S I O N
of the Technical Board of Appeal 3.5.01
of 18 July 2007

Appellant: Compaq Computer Corporation
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 11 June 2003 refusing European application No. 98308284.3 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: S. Steinbrener
Members: K. Bumes
G. Weiss

Summary of Facts and Submissions

I. This appeal is against the decision of the examining division to refuse European patent application 98308284.3, published as

A1: EP-A1-0 911 736,

on the ground that the method of claim 20 lacked novelty over document D2 (Article 54 EPC). In addition, the examining division commented *inter alia* that the system of claim 1 lacked an inventive step over a combination of D2 and D1 (Article 56 EPC).

D1: A. Saulsbury, F. Pong and A. Nowatzyk, "Missing the Memory Wall: The Case for Processor/Memory Integration". Proceedings of the 23rd Annual International Symposium on Computer Architecture (ISCA '96), Philadelphia, May 22 - 24, 1996. ACM/IEEE, New York, USA, May 1996, Vol. 23, pages 90-101.

D2: A. Nowatzyk, G. Aybay, M. Browne, E. Kelly, D. Lee and M. Parkin, "The S3.mp Scalable Shared Memory Multiprocessor", Proceedings of the Twenty-Seventh Annual Hawaii International Conference on System Sciences (HICSS-27) 1994, Wailea, HI, USA, 4-7 January 1994, Vol. I: Architecture, IEEE Computer Society Press 1994, Los Alamitos, CA, USA; pages 144-153.

II. The appellant requests that the decision under appeal be set aside, the case be remitted to the department of first instance for further prosecution, and the appeal fee be reimbursed.

In the alternative, the appellant requests that a patent be granted on the basis of amended claims 1 to 34 as filed with a letter received on 13 July 2007, with claim 20 further amended at oral proceedings

before the Board on 18 July 2007.

Claim 1 reads:

"1. A multi-processing system comprising a shared memory (13) and a plurality of multi-processor nodes (10) coupled via a switch (15), each of the plurality of multi-processor nodes (10) further comprising one or more processors (12), the multi-processor system comprising:

a portion of the shared memory (13) located in each multi-processor node (10) and apportioned into a plurality of blocks;

a directory (140) in each node (10) having a plurality of entries corresponding in number to the plurality of blocks (M) of shared memory (13), each entry in the directory (140) identifying which of the plurality of multiprocessor nodes (10) stores copies of the data block; and characterised by

a serialisation point (17) coupled to the directory (140) for ordering accesses to the plurality of blocks (M) and for maintaining strict serialisation order over commands issued in response to directory accesses such that said accesses are perceived to be in order by the or each processor (12) of said multi-processor nodes (10) and allowing the processors of said multi-processing system to concurrently execute multiple references to each of the plurality of blocks (M);

a virtual channel (Q1) interconnecting the or each processor (12) of the multiprocessor nodes (10) and in which the issued commands travel in strict serialisation order; and

a victim cache (124) for providing temporary storage of victim data as it is written back to memory (13)."

III. *Procedure before the examining division*

(a) The primary examiner acting on behalf of the examining division issued a first substantive communication (6 December 2001), based on the application documents as originally filed, and cited three prior art documents (D1, D2, D3). Besides a non-unity objection (Article 82 EPC), the examiner considered that D1 took away the novelty of independent claim 19 and D2 anticipated independent claims 1 and 20. The additional subject-matter addressed by most of the dependent claims was regarded as unclear and the technical effect achieved by said subject-matter was qualified as "merely not understandable".

(b) In response to that communication, the applicant filed an amended set of claims (22 May 2002) and argued that neither D1 nor D2 taught or suggested a specific feature (serialisation point coupled to a directory) of the claimed multi-processing system and method.

(c) With a second communication (4 February 2003), the examining division summoned the applicant *ex officio* to oral proceedings (scheduled for 30 April 2003) and provided a detailed analysis of the teaching of D2 which was considered to take away the novelty of independent claims 1 and 20. The examining division introduced five additional prior art documents D4 to D8, D4 to D7 being scientific papers and D8 being a prior European patent application pursuant to Article 54(3) EPC. As D4 referred to D5 and D6, it was presented as defeating the novelty of claims 1 to 11, 14 to 16 and 19 to 32. D7 was also said to anticipate the subject-

matter of those claims. D8 was said to take away the novelty of independent claims 1 and 20 and of dependent claims 2 to 5 and 21 to 24.

(d) The applicant replied (13 February 2003) that the objections raised in the summons should have been raised in an examination report according to Article 96(2) EPC because a full examination of the application with regard to novelty and inventive step had not previously been carried out and therefore the applicant had had no opportunity to present comments within the meaning of Article 113(1) EPC.

The applicant considered that it was unreasonable of the examiner to cite five new pieces of prior art while setting a date for oral proceedings which was only ten weeks away. These five documents needed to be considered in detail and, given that the client was in the USA, this was a considerable burden in such a short time. It should be borne in mind that the applicant had no opportunity to extend the time limit for considering and responding, whereas a communication under Article 96(2) EPC would provide such an opportunity. Article 96(2) EPC required the examining division to invite the applicant as often as necessary to file his observations in writing. Hence, the examiner was requested to consider reissuing his objections in the form of an examination report.

(e) The examining division maintained the date appointed for oral proceedings and explained its reasons for doing so in a telephone consultation with the applicant's representative (17 February 2003): Firstly, the lack-of-novelty objection based on D2 had already

been raised in the first substantive communication. Secondly, documents D4 to D7 jointly referred to a single system of distributed shared memory and originated from the "inventors" [correct: the original applicant] of the present application; therefore the prior system was known to the applicant and should have been cited by him according to Rule 27(1)(b) EPC.

The applicant's right to be heard was ensured since he had the possibility of filing new claims and attending the oral proceedings as scheduled.

(f) The applicant maintained his request that the proceedings be continued in writing in view of the complexity of the technical field (27 March 2003). He nevertheless filed an amended claim 1 and provided a substantive discussion of documents D2 and D4 to D8, all of which were said not to anticipate the present invention.

(g) In another telephone consultation (11 April 2003), the primary examiner raised an obviousness objection (Article 56 EPC) to claim 1 then on file, based on a combination of D2 and D1.

(h) The applicant announced by phone (22 April 2003) that he would not attend oral proceedings. On the same day, he filed an amended claim 1 and again requested a postponement of the oral proceedings, for the reasons set out in his previous letters and also in view of the fresh obviousness objection raised by the examiner on 11 April 2003.

(i) The examining division maintained the date appointed for oral proceedings and informed the applicant accordingly (29 April 2003).

(j) The examining division held oral proceedings in the applicant's absence (30 April 2003) and decided to refuse the application pursuant to Article 97(1) EPC for lack of novelty.

In its reasons for the decision (11 June 2003), the examining division based its objection on D2 which was considered to anticipate the method according to claim 20. The examining division additionally commented on the system according to claim 1 which was considered to lack an inventive step over a combination of D2 and D1. Documents D4 to D8 were only mentioned *obiter* in a closing statement (point 4) of the reasons.

IV. The Board summoned the appellant to oral proceedings and annexed preliminary observations.

(a) The Board noted that discussion might be necessary as to whether the examining division was obliged to send a third communication (in addition to its first communication and summons), or whether the applicant's difficulty arose from a deficiency of the application as filed.

(b) Besides a number of clarity problems, the application appeared problematic in that it provided little intermediary disclosure between the general opening portion of the application and the detailed description of embodiments. To comply with Article 123(2) EPC, an amending feature could be extracted from an embodiment

only where the overall disclosure justified a generalising isolation of the feature.

(c) As to the requirement of inventive step, the Board noted that it might have to be discussed whether or not a chronological serialisation constituted a skilled person's natural approach in a situation where a data block in a memory was to be accessed by multiple processors. Correct results were more likely to be achieved by a chronological handling of memory requests than by any other conceivable order.

V. Oral proceedings before the Board took place as scheduled (18 July 2007). The appellant's arguments can be summarised as follows.

(a) The examining division's conduct of the proceedings effectively deprived the applicant of his right to be heard, at least of his right to a complete examination in writing as laid down in Article 96(2) and Rule 51(3) EPC. Prior art documents (in this case D4 to D8) in a complex technical field should not be introduced by way of a short-term invitation to oral proceedings but in a communication pursuant to Article 96(2) EPC to allow the applicant sufficient time to respond in writing. As the application had been transferred twice during prosecution, it was difficult to obtain the inventors' comments on substantive issues at short notice. Prior to its summons, the examining division had not even provided a reasoned statement with respect to D2 which the division alleged to be novelty-defeating.

(b) The multi-processing system according to the amended claim 1 derives from the original version of claim 1 by

adding features from the description in a logical manner: The serialisation function is defined more precisely as allowing each processor to perceive memory accesses in order (based on A1, paragraphs 0026 and 0170, for example). A virtual channel technique is clearly disclosed as a second aspect of the system design (e.g. paragraph 0074). The same applies to the use of a victim cache (e.g. paragraph 0081). While the application describes those aspects together with other features, it is clear from the application that the other features are optional. For example, paragraph 0079 describes a Duplicate Tag store (DTAG 20) and an Input/Output Processor tag store (IOP tag 14b) in conjunction with the directory (140) but paragraph 0085 makes clear that such tags are only needed (as fine directories in addition to the coarse directory 140) if a processing node comprises more than one processor. It is clear to the skilled reader that other features such as a transaction tracking table (TTT, paragraph 0081) are inessential to the serialisation concept. Not all the features are disclosed at the same level of abstraction, see e.g. the relatively general presentation of the invention provided in paragraph 0017 which does not mention transaction tracking tables.

(c) The available prior art does not teach or suggest the use of a serialisation point set up to maintain a strict serialisation order over commands issued in response to directory accesses as defined in paragraph 4 of claim 1. On the contrary, D2 explicitly states that the interconnect system of the shared memory multi-processor S3.mp "does not preserve order" (page 151, right-hand column, second paragraph).

The claimed serialisation of commands does not necessarily result in a chronological order. The serialisation concept of claim 1 is more general and nevertheless enables the processors of the multi-processing system to concurrently execute multiple references to the memory blocks.

Thus, the application focuses on a serialisation concept even though the description may appear to aim at cache coherency in general.

VI. The Board pronounced its decision at the end of the oral proceedings.

Reasons for the decision

Requests for remittal to the department of first instance and for reimbursement of the appeal fee

1. Pursuant to Article 10 RPBA, a Board shall normally remit a case to the department of first instance if a fundamental deficiency is apparent in the first instance proceedings. Moreover, in case of an allowable appeal, a reimbursement of the appeal fee can be ordered where the Board deems such reimbursement to be equitable by reason of a substantial procedural violation (Rule 67 EPC).

2. In the appellant's opinion, a gross procedural violation occurred in that the examining division used a short-term invitation to oral proceedings to introduce five additional prior art documents (D4...D8) in a complex technical field. Instead, the examining

division should have issued another communication pursuant to Article 96(2) and Rule 51(3) EPC to safeguard the applicant's right to be heard according to Article 113(1) EPC. The appellant referred to decision T 802/97 to support his point of view.

3. However, decision T 802/97 relates to a different situation, namely a refusal after a single substantive communication without summons to oral proceedings. The Board notes that the fundamental relationship between Articles 96(2) and 113(1) EPC has been set out in decision T 951/92 (OJ EPO 1996, 53, point 3(v) of the reasons): "In the context of the examining procedure under Articles 96 and 97 EPC, Article 113(1) EPC is clearly intended to ensure that before a decision refusing an application for non-compliance with a requirement of the EPC is issued, the applicant has been clearly informed of the essential legal and factual reasons on which the finding of non-compliance is based, so that he knows in advance of the decision both that the application may be refused and the legal and factual reasons why the application may be refused; furthermore, before issue of a decision, the applicant must have a proper opportunity to comment upon such reasons, and if he wishes, to give counter-arguments and reasoning in support of the allowance of the application, and/or to propose amendments to the application so as to avoid refusal of the application."

4. The Board holds that the applicant had a proper opportunity to comment on the legal and factual reasons for which the examining division refused the application.

4.1 The examining division considered the method of claim 20 (in the text then on file) to be anticipated by D2. That objection and that prior art document had been put forward briefly in the examining division's first substantive communication (6 December 2001, point 2.2) and then extensively in its summons (4 February 2003, point 1.1).

The decision under appeal mentions the prior art documents D4 to D8 only *obiter.* Those documents, while cited in the summons, did not therefore play a decisive role. However, even if they formed part of a critical argumentation, the Board would not necessarily consider their late introduction through summons as improper.

4.2 In the Board's judgment, the time frame for the applicant to respond to the examining division's summons was appropriate. A time limit of two and a half months is in conformity with Rule 71(1) EPC and is not considered unduly short by the Board. The 2-month minimum provided for by Rule 71(1) EPC already takes account of potential international communication hurdles (which tend to vanish anyway owing to modern communication technology).

The present application may be difficult to process by any applicant or representative because the disclosure leaves the reader wondering about the teaching of the application (see point 7 *infra*). However, no right to a special treatment (e.g. a postponement) could be derived from a deficiency of the application.

Apart from the non-extendable time limit, the appellant had an opportunity to respond to the summons in writing

as if he responded to a communication under Article 96(2) EPC. He actually did so by submitting amendments and arguments with his letter dated 27 March 2003 which dealt with all the prior art documents D1 to D8.

4.3 Oral proceedings can be arranged at the instance of the EPO if it considers this to be expedient (Article 116(1) EPC). In particular, clarity problems can be handled expediently during oral proceedings, and the present application does involve clarity problems, with respect to both its claims and disclosure.

In its summons to oral proceedings, the examining division gave a detailed analysis of document D2 and indicated why a refusal was imminent in the light of this document. Prior to the oral proceedings, several telephone consultations informed, and warned, the applicant about the examining division's negative position.

The oral proceedings before the examining division presented an opportunity for the applicant to counter at least the line of argument based on D2, irrespective of the significance that other documents might assume during the oral proceedings. If documents D4 to D8 had been discussed at the oral proceedings and their relevance had not become clear, the applicant could have requested that the examining division continue the procedure in writing. However, the applicant decided not to participate in the first-instance oral proceedings.

5. Hence, the Board judges that no procedural violation occurred on the part of the examining division which would justify a remittal of the case or a reimbursement of the appeal fee.

Admissibility of amendments

6. A European patent application may not be amended in such a way that it contains subject-matter which extends beyond the content of the application as filed (Article 123(2) EPC).

To comply with that requirement, an amending feature can be extracted from an embodiment only where the overall disclosure justifies a generalising isolation of the feature. Where elements contributing to a subject of the application (here: cache coherency) are presented indiscriminately, those elements *prima facie* cannot be incorporated selectively in an amended claim unless the skilled reader identifies the omitted elements as inessential (cf. decision T 404/03).

7. *Content of the application as filed*

The application as filed describes a multi-processor computer system sharing a distributed memory. The application is problematic in that it provides little intermediary disclosure between the general opening portion of the application (see A1, paragraphs 0001...0019) and the detailed description of embodiments. Moreover, even the most general portions of the description do not match the independent claims as filed.

7.1 The application mentions numerous problems at some 30 places of the description, see paragraphs 0004, 0007 to 0014; brief description of Figures 26, 28A-28B, 29, 31, 33A-33B, and 34; paragraphs 0025, 0073, 0107, 0206, 0207, 0219, 0220, 0254, 0259, 0287, 0293, 0295, 0306, 0313, 0324, 0333, and 0340.

It is not transparent what the relative importance of all these problems is, which of the problems are tackled by the independent claims, to what extent the problems are solved by the claimed features, and which features are essential/sufficient to solve the problems. The Board notes that the appellant himself qualifies the field of the application as complex. All the more a structured presentation of its teaching would have been necessary.

7.2 The description mosaic conveys the overall impression that cache coherence (or coherency) is the central concern of the application, see paragraphs 0007 to 0010, 0013, 0017, 0021, 0022, 0024, 0025, 0058, 0067, 0070, 0071, 0074, 0078, 0079, 0093, 0097, 0099 to 0102, 0105, 0134, 0158, 0160, 0164 to 0166, 0168, 0169, 0174, 0181, 0203, 0206, 0215 to 0218, 0220, 0221, 0223, 0225 to 0227, 0240, 0254, 0260, 0261, 0268, 0269, 0272, 0285 to 0287, 0292, 0293, 0296, 0306, 0308, 0312, 0313, 0338 to 0340, and Figures 23, 27A to 27C, 30 and 31.

It is not entirely clear from the application which of those features relating to cache coherence are optional. The description presents the coherence-related aspects indiscriminately. A number of techniques are said to maintain cache coherency but the independent claims recite only part of those techniques, leaving some

cache coherency problems unresolved. For example, a mere serialisation of directory and memory accesses does not prevent ambiguities (see paragraphs 0268, 0287, 0295, 0301, 0306, 0308).

7.3 Independent claims as filed (A1: system claims 1 and 19, method claim 20) normally represent a reader's starting point where he expects an application to define the most general principle(s) of a solution to the most general problem underlying the application. However, cache coherence is not mentioned by any of the claims.

7.4 Moreover, the independent claims as filed do not correspond to the general opening portions of the description which the reader would expect "to disclose the invention, as claimed, in such terms that the technical problem (even if not expressly stated as such) and its solution can be understood" (Rule 27(1)(c) EPC).

For example, the independent claims do not match the applicant's global goal stated in paragraph 0014, and the independent claims differ from the solution presented in paragraph 0017.

7.5 Some generality may be gathered *prima facie* from a middle part of the description, paragraphs 0071 and 0074, which emphasise two of "several aspects" of the cache coherent NUMA [Non-Uniform Memory Access] architecture: message ordering and virtual channels, respectively. However, the ensuing description again provides no intermediary disclosure but presents a body of implementing details which all have technical significance in the cache coherency architecture and protocol.

8. *Amendments to claim 1*

Original system claim 1 relates to a multi-processing system comprising a shared memory, a directory and a serialisation point to allow multiple simultaneous references to each data block of the shared memory.

To form the amended claim 1 received on 13 July 2007, in substance the following features have been added to claim 1 as filed.

8.1 The serialisation point is specified as maintaining strict serialisation order over commands issued in response to directory accesses such that said accesses are perceived to be in order by the or each processor of said multi-processor nodes.

8.2 A virtual channel interconnects the or each processor of the multiprocessor nodes and allows the issued commands to travel in strict serialisation order.

8.3 A victim cache provides temporary storage of victim data as it is written back to memory.

9. *Admissible amendments*

The description addresses the aforementioned features as part of the cache coherence strategy.

9.1 Although the serialisation point plays a key role in the original claim 1 (and in the appellant's argumentation), the disclosure of what the serialisation point actually is and does is scarce and

scattered across the description (paragraphs 0017, 0018, 0026, 0079, 0101, 0102, 0170, 0171, 0173, 0205, and 0261). Since the basis of disclosure is small in that respect, modifications can easily extend beyond the teaching of the application as filed.

While the reader gets the impression that each multi-processing node has a serialisation point in the form of a bus (see the above-mentioned paragraphs), the appellant has chosen to define the serialisation point in claim 1 in functional terms. Functions of the serialisation point are originally disclosed in paragraphs 0017 (lines 23 to 25), 0018 (lines 47 to 49), 0026 (lines 41 to 43), 0101 (lines 55 to 57), 0170, and 0173.

The amended claim 1 amalgamates those original functional definitions and specifies *inter alia* that the serialisation point is for maintaining strict serialisation order over "commands" issued in response to directory accesses such that said accesses are perceived to be in order by the or each processor (12) of said multi-processor nodes (10).

The fact that the processors issue not only requests but also other types of commands (probes, responses) is disclosed in paragraphs 0174 to 0178.

9.2 Virtual channels and their functions are disclosed in paragraph 0074, for example, as a second aspect of the cache coherent architecture. A detailed description of virtual channels is provided from paragraph 0216 onwards. Therefore, the Board has no doubt that the features specified in the penultimate paragraph of

amended claim 1 are disclosed.

9.3 A victim cache and functions thereof are disclosed in paragraphs 0017, 0081, 0083, 0084, 0199, 0201, 0339, and original claim 19. Therefore, the Board has no doubt that the features specified in the last paragraph of amended claim 1 are disclosed.

10. *Extension beyond the content of the application as filed*

The Board holds that the incorporated features, albeit disclosed as such, have been isolated in an arbitrary manner from the overall disclosure of the cache coherent memory access architecture. At least one feature has been omitted although its function is presented as essential to achieving cache coherency.

According to paragraph 0079, several elements are provided in each of the multi-processing nodes for implementing coherent data sharing using channels, and these elements include the directory, a Duplicate Tag store (DTAG), an Input/Output Processor tag store (IOP tag), and a global port. Paragraph 0081 goes on to state that the global port includes *inter alia* a transaction tracking table (TTT) and a victim cache. The TTT keeps track of outstanding transactions (see paragraph 0082).

Paragraph 0100 expresses that the directory, DTAG, IOP tag and TTT each are used to maintain cache coherency.

Paragraph 0268 states that a number of techniques - strict ordering of Q1 channel commands, Clean-To-Dirty

(CTD) disambiguation, Shadow Commands, Fill Markers and Delayed Victim Write Buffering - are used to help the system maintain serialization order and concomitantly maintain data coherence. These techniques are used in parallel to avoid ambiguities (Figures 28A/28B, Figure 29, paragraphs 0287, 0295, 0301, 0306, 0308) and to prevent incoherent states (paragraphs 0313 to 0322). Fill markers (also mentioned in paragraph 0017) allow a processor to determine the serialisation order that occurred at the directory (paragraph 0316). The transaction tracking table (TTT) interacts with the fill markers (see e.g. paragraph 0322).

Paragraph 0339 confirms that each of the multi-processor nodes includes a victim cache, a directory and a transaction tracking table.

While the victim cache has been incorporated in the amended claim 1, the transaction tracking table (TTT) has been omitted even though it is consistently presented as a prominent feature of the cache coherency architecture. Therefore, when supplementing claim 1 by features from the description, the transaction tracking table would have to be included. In the absence of that feature, the amended claim 1 represents a solution which does not derive directly and unambiguously from the application as filed.

11. *Appellant's arguments*

11.1 The appellant argues that the focus of the application is not on cache coherency in general but on serialisation in particular so that not all aspects of cache coherency are essential to the claimed concept.

However, even the most general description of the serialisation aspect (paragraph 0071: message ordering) is presented as part of the cache coherency architecture. It is true that claim 1 as filed is silent on cache coherency but that only means that the broad original version of the claim is not supported by the description (Article 84 EPC; T 409/91, OJ EPO 1994, 653). As the claim has been amended from the description, the thrust of the description cannot be ignored without infringing in particular Article 123(2) EPC.

11.2 The appellant refers to paragraph 0017 in the introductory portion of the description, which does not mention a transaction tracking table (TTT), to show that the application does not present a TTT as an essential feature.

However, the fill marker mechanism mentioned in paragraph 0017 (lines 38 to 42) depends on a transaction tracking table (see e.g. paragraph 0314 to 0320) or on an alternative component (processor and/or directory) assuring the function of a transaction tracking table (see paragraph 0321). The fact that an alternative implementation of the function is mentioned does not mean that the function is inessential.

Above all, if paragraph 0017 were to represent the teaching of the application, claim 1 would have to be directed at the features and mechanisms described in that paragraph. As claim 1 is far from reflecting those features, the claim would still be objectionable under Article 123(2) EPC.

11.3 Another argument put forward by the appellant is that the reader of the application can logically combine pieces of information from various places of the description to draw conclusions about the relative importance of features.

It is true that an inventor may be able to explain today what the nucleus of his invention was and how the various features of the description were meant to be arranged around that nucleus at the time of drafting the application. For example, it may be plausible today that a Duplicate Tag store (DTAG 20) or an Input/Output Processor tag store (IOP tag 14b) might not be necessary in special degenerated circumstances (when a "multi"-processor node has only one processor). However, the teaching of an application is not allowed to be enhanced after the filing date.

Regarding the application as filed, it is not the task of the reader (skilled person, member of the public, examining division, board of appeal, national court) to go through a data mining exercise in an attempt to extract a general concept from a bottom-up type of disclosure. If a general concept is intended to be claimed, it has to be made available by the application.

12. The Board judges that the skilled reader of the application as filed does not identify the claimed combination of features as a solution to an identifiable problem. The general teaching of claim 1 as amended cannot be gathered from the application as filed, contrary to the requirements of Article 123(2) EPC. Hence, claim 1 is not allowable for that reason.

Article 56 EPC - Inventive step

The following substantive comments may be added.

13. Claim 1 is drawn up in a two-part form (see point II *supra*), the preamble reflecting features of the multi-processing system which are jointly known from D2. With respect to the characterising part of the claim, the appellant alleges in particular that D2 fails to disclose a serialisation point because D2 states that its "interconnect system does not preserve order" (D2, page 151, right-hand column, paragraph 2).

However, when that statement is read in the context of D2, it becomes clear that it just refers to the use of virtual channels and a typical property of virtual channels: they are packet switched, i.e. data packets forming a message do not have to be transferred in a chronological order but they may be realigned at their destination (cf. D2, page 144, left-hand column, "Introduction"; page 148, left-hand column, "Deadlock avoidance").

The present application likewise uses virtual channels (A1, page 26, line 20) to avoid deadlocks (A1, e.g. paragraph 0074) and also acknowledges that data packets may not be ordered (A1, paragraph 0277).

Hence, the above-mentioned statement in D2 does not invalidate the examining division's finding that the multiprocessor system according to D2 orders references to a shared memory block as they are received at a serialisation unit.

14. From a technical point of view, a chronological serialisation represents a skilled person's natural approach in a situation where a memory block is to be accessed by multiple processors. Correct results are more likely to be achieved by a chronological handling of memory requests than by any other conceivable order. A non-chronological order is *prima facie* likely to create chaos.

It is true that serialisation does not necessarily mean a chronological order but a chronological order certainly establishes a serialisation and thus falls within the definition of claim 1. Apart from the (conventional) use of virtual channels, the application is silent on how to implement any non-chronological serialisation.

The Board concludes that the serialisation feature as claimed is either implicit to the teaching of D2 or at least obvious from general considerations.

That finding is corroborated by the application itself (paragraph 0170): "Most [sic] prior art protocols for large SMP systems do not have this property [serialisation of loads and stores] and are consequently less efficient and more complex." This statement implies that some prior art protocols do provide for serialised memory requests as described and claimed by A1.

15. As mentioned above, a virtual channel technique is disclosed by D2 (see page 148, left-hand column, chapter "2.3 Deadlock avoidance") and, thus, does not

constitute a novel feature.

16. While a victim cache is not mentioned by D2, the use of a buffer for "victimized data" (A1, paragraph 0083) that is to be written back to memory is well-known in the field of multiprocessor systems, see D1, page 95, right-hand column, chapter "5.4 Adding a Victim Cache". D1 teaches that even a small buffer works to "increase the effective associativity of the cache in cases where the cache miss rate is dominated by conflicts, reducing the number of main memory accesses."

Such advantages induce the skilled person to use a victim cache also in the multiprocessing system of D2. The appellant has not asserted any specific adaptation of his victim cache, nor does claim 1 deal with any such adaptation.

17. Therefore, in the Board's opinion the multi-processing system according to claim 1 would not involve an inventive step over the teaching of D2, contrary to the requirements of Article 56 EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

T. Buschek S. Steinbrener