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D E C I S I O N
of 25 January 2006

Case Number: T 1148/03 - 3.5.02

Application Number: 96928894.3

Publication Number: 0846371

IPC: H03K 19/20

Language of the proceedings: EN

Title of invention:
CMOS buffer circuit having power-down feature

Applicant:
FUJITSU LIMITED

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
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Case Number: T 1148/03 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 25 January 2006

Appellant: FUJITSU LIMITED
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 6 February 2003 refusing European application No. 96928894.3 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: J.-M. Cannard
C. Holtz

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division to refuse European patent application No. 96 928 894.3. The reason given for the refusal was that the subject-matter of claims 1 to 3 filed with the letter of 1 October 2002 did not involve an inventive step within the meaning of Article 56 EPC.

II. The document:

D1: Patent Abstracts of Japan, vol. 10, No. 1 (E-371), 7 January 1986 & JP-A-60 165 119,

considered in the first instance proceedings, remains relevant to the present appeal.

Another piece of prior art:

D9: "I_{DDQ} Testing on a custom automotive IC", Shobha R. Mallarapu et al, IEEE 1994 Custom Integrated Circuits Conference, pages 405 to 408,

mentioned in a communication from the Board annexed to summons to attend oral proceedings, is considered in this decision.

III. The current version of claim 1, which was filed with a letter of 1 October 2002, with reference numeral (21) amended to (20), reads as follows:

"A method of testing a buffer circuit (20), the buffer circuit including:

an input node (A),

a plurality of transistors (MN_{A0}, MN_{A1}, MN_{An}) each having a control terminal (A_0, A_1, A_n) coupled to receive an associated input signal, a first current handling terminal coupled to a first reference voltage, and a second current handling terminal coupled to said input node (A);

a test terminal (22) for receiving a test signal;

a single pull-up transistor (MP_1) having a first current handling terminal coupled to a second reference voltage, a second current handling terminal coupled to said input node (A), and a control terminal coupled to said test terminal (22), said single pull-up transistor acting to pull up said input node (A) in normal operation of the buffer circuit (20);

a pull-down transistor (MN_{pd}) having a first current handling terminal coupled to said first reference voltage, a second current handling terminal coupled to said input node (A), and a control terminal coupled to said test terminal; and

an inverter (12) the input of which is connected to said input node (A), and the output (Z) of which provides the output of the buffer circuit;

the method comprising:

applying a test signal to said test terminal (22) such that no DC current flows in said buffer circuit and the

input node (A) is shorted to said first reference voltage; and

measuring the quiescent current flowing in the buffer circuit."

Claims 2 and 3 are dependent on claim 1.

IV. Oral proceedings were held on 25 January 2006.

V. The arguments of the appellant can be summarized as follows:

The CMOS circuit shown in figure 2 of the application comprised an OR logic gate followed by a buffer circuit (20) which included a pull-up transistor, a pull-down transistor and an inverter (12), all being connected to an input node (A). The transistors which formed the inverter carried large currents and were the main source of defects. They had to be tested for detecting manufacturing defects.

Document D1 disclosed a circuit which comprised an OR gate and two output transistors. It formed the closest prior art in terms of circuit structure. The control input of the circuit of D1 was used for putting the circuit in a standby mode to reduce power consumption. D1 did not disclose a buffer circuit comprising an inverter and could not be concerned with the problem of testing such a buffer circuit. An inverter could be added to the circuit of D1, but there was no hint in D1 leading the skilled person to use the standby mode for testing a buffer circuit comprising an inverter.

A circuit comprising a logic OR gate and a buffer circuit as shown in figure 2 of the application should necessarily be tested in two steps: in a first step, which corresponded to the claimed method, the buffer circuit per se was tested, and in a subsequent step, the logic OR gate was tested using the buffer circuit. During the test of the buffer circuit, a high test signal was applied to the test terminal such that all the transistors of the logic OR gate were forced into a non conductive inoperative state, the voltage at the input node (A) did not float, but was held at a zero level, and no spurious or drift voltage was present at the input of the buffer circuit so that no DC current should flow in this buffer circuit. The quiescent current flowing in the buffer circuit was then measured. D1 did not suggest a method of testing a buffer circuit, which comprised an inverter and was a part of a larger circuit, such as a logic circuit, by measuring the quiescent current flowing in this buffer circuit when the logic circuit was held in a non-operating state.

Documents D2 to D8, which had been cited by the examining division, all concerned an I_{DDQ} testing method for logic circuits, not of buffer circuits. A logic state was chosen, after which the clock was frozen and the quiescent current measured for monitoring whether the circuit worked properly in this logic state. Document D9 added nothing more to the teaching of the documents already on file.

VI. The appellant requested that the decision under appeal be set aside and that a patent be granted in the following form:

claims 1 to 3 filed with the letter of 1 October 2002, with reference numeral (21) in claim 1 amended to (20); description: pages 1 and 3a filed with the letter of 1 October 2002 and pages 2 to 6 filed with the letter of 2 January 2001; and

drawings: figures 1 and 2 as filed with the letter of 2 January 2001.

Reasons for the Decision

1. The appeal is admissible.

Scope of claim 1

2. The Board judges that present claim 1 is so worded that it covers a method of testing a buffer circuit including all the components identified in the claim up to the words "the method comprising:". Claim 1 does not merely relate, as argued by the appellant, to a method of testing a buffer circuit which consists only of a pull-up transistor, a pull-down transistor and an inverter, corresponding to the circuit part referred to by the reference sign (20) in figure 2 of the published application (WO97/08832).

2.1 It is true that in the description (page 5, lines 4 to 26), the expression "buffer circuit" refers to the circuit part (20) of figure 2, which consists only of a pull-up transistor (MP_1), a pull-down transistor (MN_{pd}) and an inverter (12) connected as shown in the figure. However, the description of the application also states:

- "During test mode, where it is desired to perform I_{DDQ} testing upon circuit 20 or the IC circuit in which circuit 20 is contained, a logic high test signal is provided to test node 22." (page 5, line 27 to 30),

- "Any quiescent current I_{DDQ} flowing in circuit 20, or in its host IC, resulting from ..., may readily be detected" (page 6, lines 7 to 11), and

- "the present invention is not limited to the specific buffer circuit 20 (Figure 2) but rather may be used to facilitate I_{DDQ} testing of any circuit which employs a such pull-up/pull-down configuration" (page 6, lines 16 to 19).

Such an IC circuit containing the circuit (20) is shown, as an example, in figure 2 of the application, and, furthermore, was the subject of claim 1 as originally filed.

2.2 Amending the reference sign relating to the expression "buffer circuit" in present claim 1 from (21) to (20) cannot change the meaning which should be given to the expression "buffer circuit" when construing claim 1 since the reference signs shall not be construed as limiting the claim according to Rule 29(7) EPC.

2.3 In the present case it is clear that, when construing claim 1, the expression "buffer circuit" should be given the meaning which is defined by the wording of the claim, which covers all the alternatives mentioned in the description.

3. The method according to present claim 1 comprises a step of applying a test signal to the test terminal (22) such that no DC current flows in the buffer circuit and the input node (A) is shorted to the first reference voltage, and a step of measuring the quiescent current flowing in the circuit. Such a method can detect manufacturing defects which have occurred in various components of the IC circuit in which the buffer circuit (20) is included, which IC circuit may include other components in addition to those recited in claim 1.

3.1 When a test signal is applied to the test terminal and the input mode (A) is shorted to the first reference voltage, all the transistors of the logic OR gate shown in figure 2 are forced into a non-conductive state, no switching occurs and no DC current flows in the circuit shown in figure 2. However, in practical reality, the quiescent power supply current can only be measured for the whole IC circuit in which this circuit is included. Such an IC circuit would usually comprise many more components than are shown in figure 2. Even if the transistors of the logic OR gate are forced into a non-conductive state when the input node is shorted to the first reference voltage, some of the input signals to their control terminals could be at a high voltage so that in the presence of certain manufacturing defects in this logic OR gate a quiescent current could flow in this gate. Neither claim 1 nor the application as a whole explains how to carry out measurement of a quiescent current flowing only in the circuit part (20). Thus, the appellant's argument, according to which claim 1 relates to a method of testing the circuit (20) per se independently of the logic OR gate which is

described in conjunction with this circuit (20), is not considered to be convincing.

Claim 1 - Inventive step

4. Document D1, which may be taken to be the closest prior art, discloses a logic circuit which has the following features in common with the buffer circuit specified in claim 1:

a node V_o,

a plurality of transistors (Q'_1 to Q'_8), each having a control terminal receiving an input signal, a first terminal coupled to a first reference voltage and a second terminal coupled to said node,

a control terminal receiving a control signal P_o to set the circuit in a normal operation or in a (standby) mode in which no current flows in the circuit and the node is shorted to the first reference voltage,

a single pull-up transistor (Q'_o) having a first current terminal coupled to a second reference voltage, a second current terminal coupled to the node and a control terminal coupled the input terminal, this transistor pulling up the node in normal operation of the circuit,

a pull-down transistor (Q_9) having a first current terminal coupled to the first reference voltage, a second current terminal coupled to the node, and a control terminal coupled to the input terminal.

5. The subject-matter of claim 1, with the meaning which should be given to it (*supra*: "Scope of claim 1"), differs from the prior art circuit disclosed in D1 in that it is concerned with a method of testing a buffer circuit including an inverter whose input is connected to the node (V_o), corresponding to the input node (A) in claim 1; and in that the method comprises the steps of applying a test signal to the control terminal controlling the (standby) mode of said circuit and measuring the quiescent current flowing in the circuit.

6. Starting from D1 and having regard to the effects provided by the claimed invention, two independent objective technical problems can be seen:

(i) improving the output characteristics of the circuit,

(ii) testing the circuit for detecting faults therein.

7. The Board, considering the teachings of D1 and D9 and the common knowledge of the skilled person taken in combination, judges that the subject-matter of claim 1 would be obvious to a person skilled in the art.

7.1 No inventive step could be recognized in adding an inverter at the output of the logic circuit shown in D1 since it is common practice in the relevant art to provide an inverter acting as a buffer at the output of a logic circuit to improve, or adapt, its output characteristics. It is observed that this addition would not change the way of controlling the standby mode of the circuit (understood as a mode in which no switching occurs).

7.2 Document D9 (see the sections Abstract and Introduction, page 405) shows that, already in 1994, i.e. before the priority date of the application, monitoring a quiescent current was a well-known test mode (I_{DDQ} testing) for detecting faults in a CMOS circuit and could be implemented by monitoring the current drawn by the circuit in a standby mode. Thus, it would be obvious to the skilled person faced with the problem of testing the circuit of D1 to consider providing a test signal at the circuit input terminal controlling the standby mode to set it in this mode, in which no DC current is supposed to flow in the circuit and the node is shorted to the first reference voltage, and to monitor the quiescent current of the circuit. This solution could be applied to the circuit known from D1, independently of whether or not an inverter was connected to the node Vo, and would result in a method which falls within the terms of claim 1, as explained above.

8. Since claim 1 according to the appellant's current request does not meet the requirements of the EPC, this request cannot be granted and the appeal must be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The registrar: The Chairman:

U. Bultmann W. J. L. Wheeler