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D E C I S I O N
of 21 July 2005

Case Number: T 0637/03 - 3.5.1

Application Number: 99202083.4

Publication Number: 0967544

IPC: G06F 7/544, G06F 9/302

Language of the proceedings: EN

Title of invention:
Digital signal processor for data having a large bit-length

Applicant:
Texas Instruments Incorporated

Opponent:
-

Headword:
Digital signal processor/TEXAS INSTRUMENTS

Relevant legal provisions:
EPC Art. 56, 84, 111(1), 113(1), 116(1)
EPC R. 67, 68(2)

Keyword:
"Support by the description - main and first auxiliary requests (no)"
"Remittal for further prosecution - second auxiliary request (yes)"
"Substantial procedural violation by erroneous assessment of prior art (no)"

Decisions cited:
J 0006/79

Catchword:
-

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Case Number: T 0637/03 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 21 July 2005

Appellant: Texas Instruments Incorporated
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted on 2 December 2002 refusing European application No. 99202083.4 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: S. V. Steinbrener
Members: K. J. K. Bumes
A. Pignatelli

Summary of Facts and Submissions

I. The appeal lies from the Examining Division's decision to refuse European application 99 202 083.4 for lack of inventive step.

The appellant requests, as a main request, that

- the decision under appeal be set aside;

- the application be returned to the Examining Division with a direction to grant a patent on the basis of a single claim ("Main Request") as filed on 9 February 2004 and corrected on 8 March 2005 to resume the claim refused by the Examining Division;

- the appeal fee be refunded.

On an auxiliary basis, the appellant requests that

- the decision under appeal be set aside;

- the application be returned to the Examining Division with a direction to grant a patent on the basis of a single claim ("First Auxiliary Request") filed on 9 February 2004, or a single claim filed on 8 March 2005 (second auxiliary request, pages 45 and 46).

(a) Claim 1 according to the main request reads:

"1. A digital signal processor comprising:

a digital multiplier (30) for multiplying data words to produce a product output;

a data memory (12) for storing a plurality N of data words said data memory holding the plurality N of digital words, said N words being stored therein with a least-significant-word thereof stored at an address location A and with a most-significant-word thereof stored at a location A+N;

addressing circuitry (14) for sequentially recalling a chain of data words from a first word-chain operand for supply to a first input of the digital multiplier (30);

an arithmetic logic unit (31) having a first input (A) connected to the product output of the digital multiplier (30), a second input (B) and an output (50);

characterised in that said digital signal processor further comprises:

a multiplier register (32) for holding a multiplicand word and connected to supply said multiplicand data word to the first input of the digital multiplier (30);

an accumulator (36) having a plurality of storage locations (AC0 to AC31) for M data words of a second word-chain operand said accumulator holding the plurality M of data words, said M words being stored therein with a least-significant-word thereof stored at an address location B and with a most-significant-word thereof stored at a location B+M, an output port

connected to the second input of the arithmetic logic unit for supplying said M data words and an input port connected to the output of the arithmetic logic unit for storing the result of the arithmetic logic unit output in a selected storage location; and

an accumulator addressing circuit (70) for sequentially selecting storage locations (AC) [sic] to AC 31) within said accumulator (36)."

(b) According to the first auxiliary request, the penultimate paragraph of the claim is supplemented by the words "receiving and" (emphasis added by the Board):

"an accumulator (36) having a plurality of storage locations (AC0 to AC31) for M data words of a second word-chain operand said accumulator **receiving and** holding the plurality M of data words, said M words being stored therein with a least-significant-word thereof stored at an address location B and with a most-significant-word thereof stored at a location B+M, an output port connected to the second input of the arithmetic logic unit for supplying said M data words and an input port connected to the output of the arithmetic logic unit for storing the result of the arithmetic logic unit output in a selected storage location; and"

(c) Claim 1 according to the second auxiliary request reads:

"1. A digital signal processor comprising:

a digital multiplier (30) for multiplying data words of a predetermined length to produce a product output;

a data memory (12) for storing a first plurality of data words of the predetermined length, said data words of said first plurality forming a first chain of data words representing a word of length greater than said predetermined length, said data words of said first plurality being stored in said memory with the least significant data word thereof stored at an address location A and with a most significant data word thereof of [sic] stored at a location A+N;

addressing circuitry (14) for sequentially recalling the data words of the first chain as a first word-chain multiplicand supplied to a first input of the digital multiplier (30) in N cycles;

a product high register (34) connected to said most significant output of the digital multiplier (30) for storing said most significant bits of the product output and for feeding the most significant bits of product output of a previous cycle to the multiplier at second and subsequent cycles;

a multiplier register (32) for holding a mutiplier word of the predetermined length and connected to supply said multiplier data word to a second input of the digital multiplier (30);

an arithmetic logic unit (31) of the predetermined length having a first input (A)

connected to the product output of the digital multiplier (30), said arithmetic logic unit receiving said product output as a first word-chain operand, a second input (B) and an output (50);

an accumulator (36) having a first plurality of storage locations (AC0 to AC15) for a second plurality of data words of the predetermined length, said data words of said second plurality forming a second chain of data words representing a word of length greater than said predetermined length, said data words of said second plurality being stored in said memory with the least significant data word thereof stored at an address location B and with a most significant data word thereof of [sic] stored at a location B+M, an output port connected to the second input of the arithmetic logic unit for supplying the data words of the second chain as a second word-chain operand to the arithmetic logic unit, and an input port connected to the output of the arithmetic logic unit for storing the arithmetic logic unit output in a second plurality of storage locations (AC16 to AC31) for words of the predetermined length as a word-chain output, said storage locations of said first plurality and said second plurality being paired to be addressable with a single pointer; and

an accumulator addressing circuit (70) to generate a pointer for sequentially selecting storage locations from said first (AC0 to AC15) and second (AC16 to AC20 [sic]) pluralities of storage locations within said accumulator (36) in successive operation cycles;

wherein in N+1 cycles an accumulated result of the product of multiplier word and the first word-chain multiplicand with the second word chain operand is stored in the second plurality of storage locations of the accumulator."

II. The Board issued a communication raising *inter alia* objections to the main and first auxiliary requests under Article 84 EPC. In relation to Articles 52(1) and 56 EPC, the prior art acknowledged in the introductory portion of the application and the following prior art documents were discussed:

D1: DE-A-41 23 186 (on which the appealed decision was based)

D2: US-A-5 657 262

D3: US-A-5 666 300

With respect to the request for reimbursement of the appeal fee, the Board noted that the appellant had not provided any explicit argument on that point and that no procedural violation by the Examining Division was apparent.

III. In a response dated 8 March 2005, the appellant filed the abovementioned second auxiliary request along with observations on the Board's communication. A schedule of amendments to the description and drawings has been suggested in conjunction with a proposal to postpone those amendments until after remittal to the Examining Division. A hearing was requested by way of precaution

if the appeal was not to continue to move forward by written procedure.

Reasons for the Decision

Main and first auxiliary requests

1. *Article 84 EPC - Clarity and support by the description*

When trying to match the claim (main or first auxiliary request) with the embodiments (Figures 1 and 5), the following objections arise.

1.1 According to lines 4 to 8 of the claim, a data memory (12) holds N digital data words. According to lines 9 to 11 of the claim, addressing circuitry (14) is provided for sequentially recalling "a chain of data words from a first word-chain operand" for supply to a first input of the digital multiplier (30).

The description (see e.g. paragraphs [0059] and [0065] of A2) specifies the first input of the multiplier (30) as the *multiplicand* input (33). The multiplicand consists of the chain of N words stored in the data memory 12, see e.g. paragraphs [0063], [0087] and [0092].

Since that relationship (multiplicand = first word-chain operand = N words held in memory 12) is not expressed in the claim, the claim is not supported by the description, contrary to the requirements of Article 84 EPC.

1.2 Lines 17 to 19 of the claim specify a multiplier register (32). According to the description, the multiplier register 32 holds a *multiplier* word (rather than a multiplicand word), see e.g. paragraphs [0063] and [0092] of A2.

The multiplier output is connected to a *second* (rather than the first) input of the multiplier 30, see e.g. Figures 2 and 5A (direct connection between multiplier register 32 and multiplier 30). The first input 33 of the multiplier 30 receives the multiplicand (from data bus 23).

As the claim is inconsistent with the description, it is not supported by the description.

1.3 Lines 20 to 29 of the claim define an accumulator (36) having a plurality of storage locations for M data words of a second word-chain operand to be outputted to the arithmetic logic unit (ALU) 31. The result from the ALU 31 is said to be stored in a selected storage location of the (second input of the) accumulator 36.

Throughout the description (see e.g. paragraphs [0026], [0038], [0042], [0043], [0044], [0048], [0060], [0063], [0068], [0070], [0072], [0073], [0087], [0091] to [0094], [0097], [0102], [0103], [0109]), the accumulator 36 is disclosed as a file of paired, or offset, accumulator registers designed to achieve desired technical effects, e.g. the addressing of two operands (e.g. one input and one output value) with a single pointer as summarised in paragraph [0097].

The paired structure of the accumulator 36 is effectively presented as an essential feature with respect to major objectives of the application (removal of bottlenecks to high speed processing [0005], [0009], [0044], [0066]; elimination of memory thrashing [0004], [0008], [0042], [0074]; capability of non-destructive data handling [0006], [0011], [0042]/[0043], [0071]).

As the claim does not reflect the paired structure and paired addressing of the accumulator (36), the claim is not supported by the description.

Hence, the Board judges that claim 1 of the main and first auxiliary requests is not allowable for lack of support by the description.

In his reply dated 8 March 2005 the appellant, apart from declaring his willingness to correct the error mentioned in point 1.2 above, did not comment on the lack-of-support objections but instead referred to the amendments made to claim 1 according to the second auxiliary request (discussed below).

2. *Articles 52(1) and 56 EPC*

2.1 While the claim (main and first auxiliary requests) must fail for the abovementioned formal deficiencies, its generality with respect to the accumulator usage also gives rise to the following substantive objection.

A technical problem underlying the application is "memory thrashing" (frequent memory stores and loads) due to a single-accumulator design which represents a bottleneck to high speed data processing, see

paragraphs [0004], [0005], [0008], [0009], [0042], [0074] of A2.

The application goes on to state that prior art designs comprise two accumulators to enable non-destructive operations (avoiding memory thrashing) when operating on single-word data (A2, paragraphs [0006], [0011]).

From that problem and prior art, a skilled reader will readily extrapolate the general idea of increasing the number of accumulators (or the number of storage locations in the accumulator) when the accumulator(s) present a bottleneck to high speed processing, e.g. when multiple-word data chains are to be processed.

As the claim is not limited to a specific implementation of said general idea, the Board does not see an inventive contribution in the mere use of plural accumulator storage locations.

2.2 Conversely, prior art document D1 which was the starting point of the Examining Division's decision to refuse the application is not considered to suggest a plural accumulator design in a multiplication processor. As the Examining Division's reliance on D1 has triggered the appellant's request for reimbursement of the appeal fee (as part of his main request), D1 and its use by the Examining Division will be analysed next.

2.2.1 In contrast to the claim of the main request, the accumulator unit 18 of D1 (Figure 3) comprises only one accumulator storage location (register 28). The Examining Division argued that the accumulator register (28) and the N+M storage locations of product memory 19

(D1, Figure 1) together could be considered as an overall accumulator having a plurality of storage locations. The skilled person would feed back, to the adder 27, the contents of the product memory 19 (rather than the content of the accumulator register 28) where circumstances made it desirable. The claimed signal processor was an equivalent of the one disclosed in D1. Thus, the claim lacked an inventive step. (See the paragraph bridging pages 3 and 4 of the decision under appeal.)

2.2.2 The Examining Division did not specify any explicit obvious circumstance which might prompt the skilled person to feed back the contents of the product memory locations to the adder (27), but merely referred to an "equivalent" solution.

However, an equivalent solution presupposes that it fulfils the same function. In the present case, the signal processor of D1 as modified by the Examining Division does not achieve a multiplication of two large numbers any more. In Figure 3 of D1, the binary coded decimal (BCD) elements q[0], q[1], ..., q[N+M-1] are the digits of the resulting product Q stored in product memory 19 and therefore differ from the partial products P(x[i], y[j]) that are fed to the accumulator 28 via the adder 27 to form accumulated partial products. Hence, feeding back the BCD elements (as suggested by the Examining Division) instead of feeding back the accumulated partial products (as described in D1) will not provide the same mathematical result.

2.2.3 The Board does not see any obvious modification of Figure 3 (D1) towards a plural accumulator design in a

multiplication processor allowing true three operand manipulation (see paragraph [0048] of A2). The single accumulator register 28 in D1 is not a bottleneck to the speed of computation. Even if it was, providing plural accumulator locations in D1 would be pointless because the goal (multiplication of large numbers) and concept (calculation of the result digit-by-digit) of D1 allow the elements q[k] of the product Q to be obtained only consecutively (for k=0, then for k=1, ..., finally for k=N+M-1) by shifting out the least significant BCD element from the (single) accumulator register 28 upon summing the partial products P(x[i], y[j]) (i+j=k) and the carry which was left in the accumulator (28) at the end of the previous cycle (k-1).

Second auxiliary request

3. *Article 123(2) EPC*

The Board is satisfied that the amended claim does not extend beyond the content of the application as filed.

3.1 The feature that addressing circuitry (14) recalls a first word-chain multiplicand in N cycles (page 45, lines 12 to 15 of the claim) can be gathered from paragraphs [0026] and [0048] of A2.

3.2 The specification of a product high register (34) (page 45, lines 16 to 20 of the claim) is based on Figure 5A and paragraphs [0031], [0059], [0062] and [0065] of A2.

Incidentally, the product high register effectively achieves a carry propagation by feeding the most

significant bits of the product output of a previous cycle to the multiplier at second and subsequent cycles.

3.3 A dual accumulator design and paired addressing thereof (paragraph bridging pages 45/46 of the claim; second paragraph of page 46) reflects a central aspect of the initial application, as discussed above (supra, point 1.3).

3.4 The feature that an accumulated result is stored in N+1 cycles (page 46, last paragraph of the claim) is based on paragraphs [0033], [0051], [0088], [0090] and [0095] of A2.

4. *Article 84 EPC - Clarity of the claim*

In the Board's view, some minor clarity issues (to be dealt with by the Examining Division) have remained in the amended claim. In particular, the following points need further consideration:

4.1 Page 45, line 4 of the claim: "plurality" should be replaced by "plurality N" to be consistent with the further use of "N" in the claim (page 45, line 15; page 46, last paragraph).

4.2 Page 45, line 10: "a most significant data word" should be replaced by "the most significant data word", and the redundant word "of" should be deleted at the end of the line.

4.3 Page 45, line 11: "location A+N" should be replaced by "location A+N-1" to determine N locations.

4.4 Page 45, line 16: "said" should be replaced by "a".

4.5 Page 45, line 18: "said" should be replaced by "the".

4.6 Page 45, line 19: "product output" should be replaced by "the product output".

4.7 Page 45, lines 22/23: "said multiplier data word" should be replaced by "said multiplier word" (see the preceding line 21).

4.8 Page 45, line 29: "plurality" should be replaced by "plurality M" for consistency with the embodiments (see e.g. paragraphs [0091] and [0092], where N=8 and M=9).

4.9 Page 45, line 36: "a most significant data word" should be replaced by "the most significant data word", and "of" should be deleted at the end of the line.

4.10 Page 45, line 37: "location B+M" should be replaced by "location B+M-1" to determine M locations.

4.11 Page 46, line 11: "(AC16 to AC20)" should be replaced by "(AC16 to AC31)", for consistency with lines 4/5 of page 46.

4.12 Page 46, line 15: "multiplier word" should be replaced by "the multiplier word".

5. *Further procedure*

As the amended claim relates to a specific accumulator design allowing pairs of storage locations to be

addressed by a common pointer, the claim goes beyond the general idea of having multiple accumulator locations. Owing to the common pointer, one of the paired storage locations can be accessed to fetch an input operand (i.e. an operand to be inputted to the ALU) while the paired location is accessed to store an output operand (i.e. an operand outputted from the ALU), thus accelerating the manipulation of operands, see paragraph [0026] of A2.

5.1 Prior art document D1, as discussed in detail above (point 2.2), suggests neither a plural accumulator design in a multiplication processor nor circuitry for paired addressing of accumulator locations.

5.2 Since the claim set as filed did not relate to a digital signal processor using a common pointer to address pairs of accumulator locations, that feature has not been examined yet with respect to the remaining prior art established in the search report and may not even have been subject to a search. Therefore, while said feature does not derive from D1, an assessment of the current claim (second auxiliary request) by the Examining Division is considered necessary. To this end, the Board remits the case to the department of first instance (Article 111(1) EPC).

5.3 If the Examining Division finds the claim (second auxiliary request) to be directed to novel and non-obvious matter, the claim may require further clarification as listed at point 4 above, and the description and drawings may require amendments including those proposed by the appellant in his response dated 8 March 2005 to overcome clarity issues

raised by the Board in its communication dated 10 August 2004 (points 4.5 to 4.8 therein).

5.4 Since the case is remitted to the department of first instance for further prosecution, the appellant's auxiliary request for oral proceedings before the Board need not be considered.

6. *Request for reimbursement of the appeal fee*

As part of the main request, the appellant has requested a reimbursement of the appeal fee without providing any explicit argument on that point.

6.1 A reimbursement of the appeal fee shall be ordered where the appeal is deemed allowable, if the reimbursement is equitable by reason of a substantial procedural violation (Rule 67 EPC).

A substantial procedural violation occurs only where rules of procedure have not been applied in the manner prescribed by the EPC (see J 6/79, OJ EPO 1980, 225). An error of judgement by the department of first instance is not regarded as a procedural violation (cf. Case Law of the Boards of Appeal, 4th edition, December 2001, Chapter VII.D.15.4.5).

6.2 Should the appellant's request be linked to his criticism of the Examining Division's conclusion of obviousness from an alleged equivalence between D1 and the claim, the Examining Division's assessment may involve an error of judgement but does not amount to a substantial procedural violation. The Examining Division described what it considered to be a skilled

person's path from D1 to the claimed processor. The Examining Division thus provided a reasoned decision in the sense of Rule 68(2) EPC even though the Board does not follow that reasoning in the end. The appellant (then applicant) also had an opportunity to comment on the grounds and evidence on which the Examining Division based its decision (Article 113(1) EPC); in particular, the Examining Division held oral proceedings as requested by the Applicant according to Article 116(1) EPC.

6.3 Hence, no violation of procedural rules is apparent to the Board. Therefore, the request for reimbursement of the appeal fee has to be refused.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance for further prosecution on the basis of the claim according to the second auxiliary request.

3. The request for reimbursement of the appeal fee is refused.

The Registrar: The Chairman:

D. Sauter S. V. Steinbrener