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Case Number: T 0463/03 - 3.5.01

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Title of invention:
Signal processor

Applicants:
Koninklijke Philips Electronics N.V., et al

Opponent:
-

Headword:
Signal Processor/PHILIPS

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (both requests) - no"

Decisions cited:
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Case Number: T 0463/03 - 3.5.01

D E C I S I O N
of the Technical Board of Appeal 3.5.01
of 8 September 2006

Appellants: Koninklijke Philips Electronics N.V.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 30 October 2002 refusing European application No. 97925232.7 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: S. Steinbrener
Members: W. Chandler
P. Schmitz

Summary of Facts and Submissions

I. This appeal is against the decision of the examining division to refuse the application on the grounds that claim 1 of the main and first auxiliary requests did not involve an inventive step (Article 56 EPC) over US-A-4 725 973 (D1), and that the subject-matter of the second auxiliary request did not satisfy the requirements of Rule 86(4) EPC.

II. In the statement setting out the grounds of appeal, the appellants requested that the decision under appeal be set aside and a patent be granted on the basis of claims 1 to 12 of the main or first auxiliary request, both identical to the corresponding refused requests. The appellants did not reply to the communication accompanying the summons to oral proceedings, in which the Board summarised the issues to be discussed. In particular, the Board expressed some doubts about the patentability of the claims when starting from the embodiment shown in Figure 2 of D1 and taking into account common general knowledge as exemplified by DE-A-43 44 157 (D2).

III. At the oral proceedings, although duly summoned, nobody appeared for the appellants. At the end of the oral proceedings, the Chairman announced the decision.

IV. Claim 1 of the main request reads as follows:
"A signal processor comprising
– at least one data source (3),
– at least three input registers (11, 12, 13, 14...) whose inputs are directly coupled to the data source (3) by data buses (9, 10),

— processing means (19, 20, 22, 23, 25, 26, 54-60, 62, 64, 65, 71, 72, 73) for processing data buffered in the input registers by arithmetic and/or logic operations, which processing means are spread over parallel data processing branches (4-0, 4-1, ..., 4-N), and
— multiplexing means (15, 16, 17, 18) that are provided for coupling outputs of a respective part of the input registers (11, 12, 13, 14,...) to inputs of the processing means of the various processing branches (4-0, 4-1, ..., 4-N) in dependence on control signals (I, II, III, IV)."

Claim 1 of the auxiliary request adds to the end of claim 1 of the main request the feature:

"allowing a single datum buffered in an input register to be used in parallel by a plurality of processing means."

V. In the statement setting out the grounds of appeal, the appellants argued essentially as follows:
In contrast to D1, in the present application the data source was directly coupled via data busses to at least three input registers. The selector structure 2' shown in Figure 2 of D1 required floor space, which increased the manufacturing costs of a mass-produced product.

The selector means 3' shown in D1 did not allow a single datum buffered in an input register to be used in parallel by a plurality of processing means as specified in the auxiliary request. D1 gave no hint that this selector should do more than select one of its inputs and deliver this to one input of one of the

arithmetic logic units. This was in line with the definition of a selector, which was a switch that could select one of its inputs and transmit it to one of its outputs, but not send one input in parallel to a plurality of outputs. Although a selector according to D1 distributed its inputs in parallel to its outputs, it functioned only as a cross-bar element and not a multiplexer.

Reasons for the Decision

1. The appeal complies with the requirements referred to in Rule 65(1) EPC and is, therefore, admissible.

2. The application relates to a general-purpose parallel signal processor (see Figure 2 and page 4, line 21 to page 6, line 3) that can calculate a variety of algorithms (e.g. correlation, filter and long-term prediction functions – see page 3, lines 7 to 11). It has a flexible way of distributing data to the processing units, in particular by enabling data of specific input registers (11...14) to be sent to multiple processing units (19, 20, 22, 25).

Main request

3. D1 relates to a signal processor for parallel processing of vector data, i.e. sets of data stored in a vector register 21 (see column 3, lines 5 to 16 and Figure 2). At point 13.1 of the appealed decision, the examining division interpreted D1 so that the claimed data source was the RAM 200 together with register 203', and the input registers were registers 203 and 204, all

within a single vector register 21 shown in Figure 3 of D1. However, the Board agrees with the appellants that since each vector register in D1 only has two input registers (203, 204) for each data source (200, 203'), it is difficult to argue that at least three input registers are directly coupled to the data source as claimed.

4. However, claim 1 is so broad as to allow a number of other possible interpretations of this prior art. In particular, the Board considers that a more logical interpretation of D1 is to consider the memory 5 in Figure 2 as the data source and the vector registers (VR1...VRn) as the input registers. This structure accords better with the overall operation of the invention whereby data from the memory can be sent to any of the registers. The Board considers that each vector register as a whole can be interpreted as a register in the sense of the claim since the latter is not restricted to a single storage element. Under this interpretation, at least three of the vector registers (VR1...VRn) are coupled, albeit not "directly", to memory 5 via data buses 6 and 10. Finally, the registers are connected to processing means (ALU1...ALUl) spread over parallel processing branches via selector means 3'.

5. Thus, the Board judges that the subject-matter of claim 1 differs from D1 in that:
- the input registers are directly coupled to the data source by data buses and
- the outputs of the input registers are coupled to the processing means by multiplexing means instead of selector means.

6. Since it is difficult to attribute a specific effect to these differences in such a general-purpose circuit, the Board judges that the problem solved by the distinguishing features is to find an alternative solution for distributing the information between the data source and the parallel processing means in the signal processor.

7. Regarding the use of multiplexing means instead of a selector, the Board cannot see how this involves an inventive step. Firstly, as far as the Board is aware, in electrical engineering literature the terms "selector" and "multiplexer" are often used as synonyms for the same purpose. In particular, a multiplexer is used when a selector function is required. Secondly, as far as the function of these elements is concerned, D1 does not describe exactly how the selector 3' operates, but states at column 3, line 66 to column 4, line 2 that it transfers data from the register (VR) 21 to the arithmetic logic units 4. It is not stated to be limited to sending the output from one register to only one arithmetic logic unit, nor does there appear to be any reason to do so. Thus, in order to implement this function, the Board considers that the skilled person would consider a multiplexer as an implementation of the selector in D1 at least as an obvious, if not self-evident or even identical choice.

8. Regarding the direct connection between the data source and the input registers, the Board considers that whenever multiple units (e.g. memory, registers etc.) are connected to a data bus, there must be means for selecting which unit is active (e.g. select signals).

This is implicit and can also be assumed to be present in the signal processor according to the invention. Thus, a kind of selector must be included in every unit connected to the data bus according to the invention. The Board judges that the skilled person, knowing that it is necessary to have such selection means for connecting a plurality of units to a data bus, would consider directly coupling them with data busses and selecting individual units as implicitly claimed, or using a single selector as in D1 as obvious alternatives.

9. Moreover, D2, which is from a predecessor of one of the present applicants and relates to the same field of parallel signal processing of vectors as is apparent from page 2, lines 31 to 33, indicates that this is a common technique. According to Figure 2 of D2, the input registers 11 and 12 are directly connected to the data source 3 by data buses 9 and 10.

10. The appellants considered that the selector structure 2' shown in Figure 2 of D1 required floor space, which increased the manufacturing costs of a mass-produced product. However, the Board judges that floor space is required for realising either of the above-mentioned selection mechanisms, and that the skilled person would choose one depending on the known advantages and disadvantages of each possibility.

11. The subject-matter of claim 1 of the main request accordingly does not involve an inventive step (Article 56 EPC).

Auxiliary request

12. Claim 1 of the auxiliary request further specifies that the multiplexing means allows a single datum buffered in an input register to be used in parallel by a plurality of processing means.

13. D1 states at column 1, lines 34 to 38 that selector 3' directs the output of a vector register VR as an operand to a desired arithmetic logic unit ALU. Hence, selector 3' offers the flexibility to choose to which ALU to direct an input register's output. Furthermore, D1 discloses at column 3, line 66 to column 4, line 1 that selector 3' transfers the output of the vector register VR to "arithmetic logic units" (Board's underlining), i.e. implying to more than one at the same time. Moreover, according to D1 at column 3, lines 13 to 15, the arrangement with selector 3' is said to allow for concurrent execution of a shared vector instruction by a plurality of arithmetic logic units ALU. Thus, it appears that in D1 selector 3' does indeed allow a single datum buffered in an input register VR to be used in parallel by arithmetic logic units ALU, i.e. by a plurality of processing means.

14. Regardless of whether this is the case or not, the Board essentially agrees with the examining division at point 14.2 of the appealed decision that this additional feature follows in an obvious way from the choice of the function to be carried out by the processor. In D1, each stage of calculating the function A(i)+B(i).C(i) involves different pairs of operands. However, as soon as the function involves the same pair, namely a squaring function such as in the

well-known computation of energy functions, the skilled person would immediately realise that the same datum must be provided in parallel to more than one processing means, as claimed.

15. Finally, D2 shows such a possibility in Figure 2 where the output of register 11 is connected to both processing units 13, 17.

16. The subject-matter of the auxiliary request accordingly does not involve an inventive step either (Article 56 EPC).

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

P. Guidi S. Steinbrener