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D E C I S I O N
of 27 July 2005

Case Number: T 0461/03 - 3.5.01

Application Number: 95119863.9

Publication Number: 0717350

IPC: G06F 7/52, G06F 7/552

Language of the proceedings: EN

Title of invention:
High-speed division and square root calculation unit

Applicant:
KABUSHIKI KAISHA TOSHIBA

Opponent:
-

Headword:
Calculation unit/TOSHIBA

Relevant legal provisions:
EPC Art. 83, 111(1)

Keyword:
"Sufficiency of disclosure (no)"
"Standard of disclosure - exemplified by prior art documents"

Decisions cited:
-

Catchword:
Prior art documents can demonstrate the degree of disclosure expected by a skilled person in the technical field of the application (point 4 of the reasons).

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0461/03 - 3.5.01

D E C I S I O N
of the Technical Board of Appeal 3.5.01
of 27 July 2005

Appellant: Kabushiki Kaisha Toshiba
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 19 November 2002 refusing European application No. 95119863.9 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: S. V. Steinbrener
Members: K. J. K. Bumes
B. J. Schachenmann

Summary of Facts and Submissions

I. The appeal lies from the Examining Division's decision to refuse European patent application 95119863.9 for inadmissible amendment (Article 123(2) EPC - main request) or lack of clarity (Article 84 EPC - auxiliary request).

The appellant requests that the decision under appeal be set aside and that a patent be granted on the basis of an amended claim 1 according to the main or auxiliary request filed with letter dated 5 July 2005, or, as a further auxiliary request (expressed during oral proceedings before the Board), that the case be remitted to the first instance for further prosecution.

(A) Claim 1 of the main request reads:

"1. A calculation unit having a sequence of a predetermined plurality of on-the-fly quotient digit decoders (46), for calculating a division or square root according to a radix two iteration algorithm with a quotient digit being converted from redundant form into nonredundant form, each of the on-the-fly quotient digit decoders (46) comprising:

(a) a bit position indicator (111) for storing bit positions where a quotient digit is calculated;

(b) a first quotient digits memory (112) for storing a quotient digit set of nonredundant form prepared on the assumption that there is carry propagation from a lower position;

(c) a second quotient digits memory (113) for storing a quotient digit set of nonredundant form

prepared on the assumption that there is no carry propagation from a lower position; and

(d) on-the-fly digit handling means (114) for generating nonredundant quotient digit sets according to data provided by the bit position indicator (111), the first and second quotient digits memories (112, 113) and the quotient digit in redundant form to provide a next quotient digit to another on-the-fly quotient digit decoder (46) at the next stage, wherein the calculation unit provides a nonredundant quotient digit of at least two bits in one operation."

(B) According to the auxiliary request, paragraphs (b) and (c) of claim 1 read:

"(b) a first quotient digits memory (112) for storing a quotient digit set of nonredundant form prepared on the assumption that there is carry propagation from another on-the-fly quotient digit decoder (46) at the previous stage, providing the quotient digit set at a lower bit position;

(c) a second quotient digits memory (113) for storing a quotient digit set of nonredundant form prepared on the assumption that there is no carry propagation from another on-the-fly quotient digit decoder (46) at the previous stage, providing the quotient digit set at the lower bit position; and"

II. The Examining Division raised a lack-of-clarity objection under Article 84 EPC in relation to the terms "carry propagation from a lower position" which the Examining Division considered as undefined in claim 1 (point 12 of the decision under appeal). The skilled person would have to make an inventive step to

establish where the carry propagation comes from and to find out the content of the quotient digits memories.

III. The Board summoned the appellant to attend oral proceedings and *inter alia* noted that the clarity issue presented by the Examining Division amounted to an objection under Article 83 EPC since the decision under appeal effectively qualified the disclosure of the application as insufficient.

Therefore, a discussion appeared necessary on whether or not a plausible operational scheme could be derived from the original disclosure in the light of prior art documents such a those listed in the (partial) European search report:

D1: IEEE Transactions on Computers, vol. 34, No. 8, August 1985, New York (US), pages 724 to 733, XP002000068, S. Majerski: "Square-Rooting Algorithms for High-Speed Digital Circuits".

D2: Energy and Information Technologies in the Southeast, Columbia, 9-12 April 1989, vol. 3 of 3, 9 April 1989, Institute of Electrical and Electronics Engineers, pages 1361 to 1365, XP000076647, Nienhaus H A et al.: "A Parallel SRT Divider For Systolic Linear System Solvers".

D3: Proceedings of the 7th IEEE Symposium on Computer Arithmetic, 4-6 June 1985, Urbana, IL, USA, 1985, IEEE Computer Society Press, Los Alamitos CA US, pages 51 to 56, XP002000069, M Ercegovac et al.: "A Division Algorithm with Prediction of Quotient Digits".

D4: IEEE Transactions on Computers, vol. 42, No. 2, 1 February 1993, pages 239 to 246, XP000355636, Montuschi P et al.: "Reducing Iteration Time When Result Digit Is Zero For Radix 2 SRT Division and Square Root With Redundant Remainders".

D5: US-A-5 237 525.

IV. At the oral proceedings before the Board, the appellant substantially argued that the claimed aspect of the calculation unit was sufficiently disclosed by the description centering around Figure 26, with hardware components detailed in Figures 9, 10, 18, for example, and organisational schemes exhibited in Figures 23 and 27, for example. Claim 1 (main and auxiliary requests) set out from claim 13 as originally filed and from the second aspect of the invention (page 4, line 51 of the application as published = EP-A2-0 717 350 = "A2" hereinafter). That aspect was described in greater detail in relation to the seventh embodiment (A2, pages 11/12). Unclaimed aspects had not been described in detail because those were peripheral to the invention and attributable to the skilled person's knowledge. The goal of the invention was to provide a hardware structure and principle (Figure 26: pairs of memories 112/113, 212/213, 312/313 storing two possible anticipated quotient digit sets) rather than applying that principle to a specific calculation algorithm or providing a new algorithm.

The disclosure addressed experts in a special field where high mathematical standards had to be presupposed enabling the skilled reader to put the claimed

invention into practice. The application used terminology in the usual meaning of the art as exemplified by D1. The complexity of the application (merging three priority documents) did not amount to an undue burden for the skilled person implementing the claimed teaching. Clear references (e.g. reference signs, notably from Figure 26) gave the reader a synopsis of interrelated parts of the description and drawings to obtain a full picture and understanding of the claimed aspect of the invention. Examples of how to embed the claimed calculation unit in a specific environment might be useful but were considered inessential because a hardware implementation and operating sequence of the claimed components were disclosed, an extensive overview of the background was provided by the introductory portion of the description, and any missing detail would be supplemented by common general knowledge.

Regarding the Examining Division's objection, the appellant argued that a carry propagation from a lower stage of the calculation unit was inherent to iterative division processing and was also disclosed explicitly in Figure 26 in that the partial remainder p_j comprising a carry bit (Figure 18) was fed into a block (overlap execution OVLP 131 in Figure 26) whose output influenced the calculation of dual sets of quotient digits in a handling block (PQR 224) of the subsequent stage. The hardware structure of such a handling block (PQR 114) was disclosed in Figure 10, while the operation of the overlap execution block (OVLP 131) was described in relation to Figure 15 (A2, page 8, line 40 to page 9, line 4). The dual sets of quotient digits were then stored in parallel memories (312, 313) of the

subsequent stage of the calculation unit. Hence, contrary to the Examining Division's objection, the contents of the claimed memory pairs were disclosed in a clear manner.

V. The chairman pronounced the Board's decision at the end of the oral proceedings.

Reasons for the Decision

Article 123(2) EPC - Admissibility of amendments

1. The Board is satisfied that the amended versions of claim 1 (main and auxiliary requests) do not extend beyond the content of the application as filed. Original claim 13 and the seventh embodiment (in particular Figure 26) deal with a plurality (A2, page 4, line 51; page 11, line 20) of cascaded quotient digit decoders (46) each comprising the claimed features (a) to (d) to provide a quotient digit of at least two bits in one operation.

Article 83 EPC - Sufficiency of disclosure

2. The European patent application must disclose the invention in a manner sufficiently clear and complete for it to be carried out by a person skilled in the art (Article 83 EPC).

At the oral proceedings, the Board endeavoured (i) to find out, with the appellant's help, how the invention works and (ii) to check whether or not the application

contained sufficient disclosure to this effect. However, the approach failed in both respects.

3. Carrying out an invention implies achieving the object(s) of the invention. The main object set out in the present application is to provide a high-speed calculation unit (for division and square root calculation) having a simple hardware structure (A2, page 3, lines 52/53). According to claim 1 (main or auxiliary request), the calculation unit is further required to convert quotient digits from redundant to non-redundant form during the calculation process.

3.1 On the one hand, the Board has convinced itself that a conversion of digits from a redundant (signed) form to a non-redundant (unsigned) form is a matter of routine in division processors although the application just desires such a conversion to take place rather than specifying any conversion step (A2, e.g. page 3, lines 12/13; page 4, lines 53/54; page 5, lines 21 to 23; page 7, lines 32/33; page 11, lines 12/13; page 12, lines 34/35; page 16, claim 13).

Further, it appears plausible that the cascaded plurality of quotient digit decoders provides a non-redundant quotient digit of at least "two bits in one operation" (A2, page 4, lines 54/55; page 16, claim 13). Generating two bits (minimum number covered by claim 1 of the main or auxiliary request) or four bits (embodiment 7) in one iteration step seems possible owing to the presence of two (claim 1) or four (embodiment 7 - A2, page 11, lines 10/11) quotient digit decoders (referenced "46" in Figure 9).

Another plausible partial aspect relates to the use of a pair of quotient digits memories (112/113; 212/213; 312/313) in each quotient digit decoder (46) to allow each decoder (46) to rely on one of dual results prepared for two possible events: A first prepared result is based on the assumption that a carry will arrive ("propagate") from the preceding stage, and a second prepared result is based on the assumption that no carry will arrive from the preceding stage. Once the actual carry is known, one of the prepared results can be selected appropriately and immediately.

3.2 On the other hand, the Board - like the Examining Division - has not been in a position, even with the appellant's assistance at the oral proceedings, to assess the correctness of the calculation result achieved by the claimed calculation unit. While Figure 26 may describe a central portion of a division processor (with sub-structures detailed in related Figures), the algorithm underlying its operation is not completely transparent. The contents of one memory pair (312, 313) in Figure 26 may be determined in some complex way by preceding hardwired logic gates, but any compliance of the data handling process with an iteration concept or algorithm cannot be verified because no overall concept or algorithm has been disclosed in relation to the claimed hardware structure. It is not clear how the circuit of Figure 26 is to be embedded in a complete iteration process meant to provide successive quotient digit sets. The starting values of the first quotient digits, i.e. the digit sets in the first pair of memories (112, 113), are unknown even though they are necessary to calculate the dual quotient digit sets held in subsequent pairs of

memories (212/213, 312/313). It is clear (e.g. from Figures 9, 10, 26) that the dual quotient digit sets represent non-redundant values calculated on the assumption that a carry bit propagates or does not propagate, respectively, from a previous stage of the calculation unit; however, it is not clear at what stage the iteration terminates and which of the dual quotient digit sets will be considered to be correct in the final stage. The impact of a carry propagation to the subsequent stage is obscure and its accuracy cannot be evaluated by the reader of the application. These gaps in the disclosure are not seen to be filled by the timing scheme depicted in Figure 27, and they cannot be filled by the introductory portion of the description referring to prior art approaches which are dismissed as improper, disadvantageous, problematic, slow and/or complicated (A2, page 2, lines 29/30, 37/38, 47/48; page 3, lines 3 and 8 etc).

4. The Board considers the skilled person to be a scientist in applied mathematics having knowledge of hardware circuits for implementing calculation processors. Where necessary, a team will be formed to bring those skills together which are clearly required in the technical field of the current application.

A crucial question is what degree of disclosure is expected by the skilled person in the field of hardware processors for carrying out complex iterative algorithms such as those aiming at high-speed divisions. In the Board's judgment, the available prior art documents D1 to D5 demonstrate the level of detail required, all of them including extensive background theories, in particular the algorithms used, and fully-

fledged numeric examples of the iteration on a step-by-step basis.

That standard is in sharp contrast with the disclosure of the current application which comprises neither an overarching algorithm nor a complete numeric example. The "claimed embodiment" (Figure 26) is only a fractional view of a vague overall system (Figure 23) that would require further ingenuity to accomplish a division and square rooting hardware.

5. In the Board's conclusion, an overall system and algorithm required to achieve the goals of the application cannot be devised without undue burden by a skilled person relying on the disclosure of the application and his general knowledge. Despite the appellant's attempts to read the various pieces of disclosure into a homogeneous concept and teaching, the Board's doubts about the operation and performance of the claimed calculation unit have not been overcome.

Therefore, the Board judges that the application fails to meet the requirements of Article 83 EPC, thus confirming the Examining Division's implicit insufficiency objection (point III supra). Due to this fundamental deficiency, the application cannot proceed to grant.

6. Under these circumstances, the Board exercises its discretion under Article 111(1) EPC so as to refuse the appellant's further auxiliary request for remittal of the case to the department of first instance.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Kiehl S. V. Steinbrener