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D E C I S I O N
of 8 April 2005

Case Number: T 0216/03 - 3.4.2

Application Number: 97918268.0

Publication Number: 0897554

IPC: G02F 1/35

Language of the proceedings: EN

Title of invention:
Optical Clock Division

Applicant:
BRITISH TELECOMMUNICATIONS public limited company

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 84

Keyword:
Features essential - no: alternative solutions disclosed in the description"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0216/03 - 3.4.2

D E C I S I O N
of the Technical Board of Appeal 3.4.2
of 8 April 2005

Appellant: BRITISH TELECOMMUNICATIONS public limited company
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Representative: Roberts, Simon Christopher
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Intellectual Property Department
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 2 August 2002 refusing European application No. 97918268.0 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: A. G. Klein
Members: A. G. M. Maaswinkel
C. Rennie-Smith

Summary of Facts and Submissions

I. The appellant lodged an appeal, received on 11 October 2002, against the decision of the examining division, dispatched on 2 August 2002, refusing the European patent application 97918268.0. The fee for the appeal was paid on 11 October 2002 and the statement setting out the grounds of appeal was received on 12 December 2002.

II. The examining division objected that the application did not meet the requirements of Article 84 EPC because the independent claims did not define all essential features of the invention which in its opinion were only defined in dependent Claim 8. During the examining proceedings the following documents had been cited:

D1: Lucek J K et al: "Remotely programmable routing device with optical clock division" IEEE Photonics Technology Letters, Jan. 1995, USA, Vol.7, no.1, pages 59 to 61;

D2: Kang K I et al: "Demonstration of all-optical Mach-Zehnder demultiplexer", Electronics Letters, 27 April 1995, UK, pages 749 and 750.

III. In reply to a communication of the board and after a telephone consultation with the rapporteur the appellant filed with its letters dated 11 and 15 February 2005 a set of amended claims and adapted description pages. The appellant requested that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

Claims: 1, 2 and 10 to 13 filed with its letter of 15 February 2005;
3 to 9 and 14 to 18 filed with its letter of 12 December 2002;

Description: pages 1 to 3 filed with its letter of 11 February 2005;
pages 4 to 12 of the published application;

Drawings: sheets 1/9 to 9/9 of the published application.

IV. The wording of independent claim 1 reads as follows:

"A method, using an all-optical non-linear gate (1) having a non linear element, of deriving a clock signal at a divided clock rate from an optical signal stream at a higher clock rate, the optical signal stream being formed by a sequence of optical pulses having a predetermined bit period, wherein the all-optical non linear gate (1) has a data input (I) for inputting optical data pulses, a control input (G) for receiving optical control pulses, and at least a first output port (O1) for the output of at least some of the optical data pulses, the gate (1) being configured such that if a data pulse is present at the data input (I), the ability of the gate to produce a corresponding data pulse at the first output port (01) is dependent on the presence or absence of a control pulse at the control input (G), and if a data pulse is absent at the data input (I), the absence of the data pulse causes the gate not to produce a corresponding data pulse at the

first output port (O1), the method comprising the steps of:

applying the optical signal stream to the data input (I) of the gate (1); and,

applying to the control input of the gate (1), via an optical feedback path (2,3,4) having a delay period associated therewith, optical data output from the first output port of the gate (1), the delay period being equal to an odd number of bit periods such that a signal at the divided clock rate is output at the first output port (O1) of the gate and/or another output port (O2) of the gate".

The wording of independent claim 11 reads as follows:

"A clock division circuit for deriving a clock signal at a divided clock rate from an optical clock stream at a higher clock rate than the divided clock rate, the optical signal stream being formed by a sequence of optical pulses having a predetermined bit period, the clock division circuit comprising an all-optical non-linear gate (1) having a non linear element, and an optical feedback path (2,3,4) having a delay period associated therewith, the gate (1) having a data input (I) for inputting optical data pulses, a control input (G) for receiving optical control pulses, at least a first data output port (O1) for outputting at least some of the optical data pulses, the gate being configured such that if a data pulse is present at the data input (I), the ability of the gate to produce a corresponding data pulse at the first output port (O1) is dependent on the presence or absence of a control

pulse at the control input (G), and if a data pulse is absent at the data input (I), the absence of the data pulse causes the gate not to produced a corresponding data pulse at the first output port (O1), wherein the optical feedback path (2,3,4) is arranged between the first output port of the gate (1) and the control input of the gate (1) such that data output from the first output port is applied via the feedback path to the control input of the gate (1), the delay period associated with the feedback path being equal to an odd number of bit periods such that when an optical signal stream is applied to the data input (I) of the gate (1), a signal at the divided clock rate is produced at the first output port (O1) of the gate (1) and/or another output port (O2) of the gate (I)".

Claims 2 to 10 and 12 to 18 are dependent claims.

V. The appellant's arguments may be summarised as follows:

Amended Claim 1 now includes functional features to specify the all-optical gate of previous Claim 1. Support for these features can be found at page 4, line 17 of the description. The functionality of the gate is also included in Claim 1, support for which can be found at page 4, line 23, where it is disclosed that the fibre loop mirror of the non-linear optical gate "directs a signal received to the input to one or other of the two output O1, O2, depending upon the presence or absence of a control signal at the input G". The feedback path is (2,3,4) and is also specified, this path having a delay period associated therewith, see page 4, lines 20 and 26, and Figure 1. Support for a signal at a divided clock rate being output at the

first output port and/or another output port of the gate can be found at page 5, line 4, where it is stated that an output at half the bit rate of the input stream is produced at output O2, and at page 5, line 26, where it is shown that the other output O2 provides a divided clock rate. This is described generally at page 5, lines 6 to 29, and can be seen graphically illustrated in the pulses a, b, c, d output from outputs O1 and O2 in Figure 1. Claim 2 is directed to a situation where an output at the divided clock rate is produced at the second output, this being supported for the reasons given in connection with Claim 1. Claim 11 is an apparatus claim corresponding to method Claim 1 and equally supported by the description. The remaining claims correspond to the same-numbered claims as filed. The amendments are thus believed to meet the requirements of Article 123(2) EPC.

In its decision the examining division expressed its view that the features of Claim 8 as filed, i.e. use of a semiconductor optical amplifier (SOA), driven with the optical signal stream at a bit rate generally corresponding to the e^{-1} recovery rate of the SOA are essential features of the invention where the delay of the feedback path is an odd number of bits, and that without these features at least Claims 1 and 11 do not meet the requirements of Article 84 EPC. However, it is made clear at page 3, lines 1 to 14 of the description that there are three alternative ways of configuring the clock division circuit. Firstly, it is stated that when the optical feedback path is equal to the period between bits in the optical signal stream, "then in response to an input stream of the form 111111, the output of the gate is in the form 101010101010". It is

then stated that "alternatively, when the total length of the delay is greater than one bit period", an initial phase of programming may be used, and that "as a further alternative", an SOA may be used, in which case the bit rate of the input stream will generally correspond to the exponential recovery rate of the SOA. It is therefore clear that if (a) the delay time through the feedback loop is more than one bit period, then either (b) the circuit needs to be initialised, or (c) an SOA is used in a regime where spontaneous clock division occurs. The fact that the use of a semiconductor amplifier in the regime where spontaneous clock division occurs is an alternative to the use of an initialisation phase is also emphasised in the specific description, such as at page 5, lines 29 and 30 and page 6, line 18, each alternative being possible even when the delay is an odd number of bit periods (see page 5, line 8 and page 6, line 21). In addition, from page 5, lines 5 to 8 the skilled person will understand that neither initialisation nor spontaneous clock division are needed when the delay is one bit period. Thus, it is clear from the description that solutions other than the use of a SOA driven at its exponential recovery rate are envisaged, namely the use of a programming phase or a single bit delay and that the features of Claim 8 are not essential to the invention.

As to patentability, in document D1 there is described a routing device for routing data at the input port to a first or a second output port. This routing device is a two stage device, having a gate as a first stage whose output is connected to the input of a clock recovery circuit acting as a second stage of the

routing device. Claims 1 and 11 are novel over D1, since in D1 it is the output of the clock recovery circuit that is fed to a control input of the gate whereas, in the present invention, the output of the gate itself is fed back to the control input. This is a material difference, since the presence of the clock recovery circuit in D1 means that there is only an arbitrary relationship between the data output of the gate and the clock recovery output that is applied to the gate control input. For example, with reference to Figure 2 in D1, the data output D of the gate may be 00010, whilst the clock recovery output at F and the signal at the control input C will remain 11010. Hence in D1 the data outputted from the gate is not applied to the control input of that gate. Furthermore, it is impermissible to construe the non-linear gate of the claims as including both stages of the routing device of D1. This is because the non-linear gate is specified as being "configured such that …if a data pulse is absent at the data input, the absence of the data pulse causes the gate not to produce a corresponding data pulse at the first port". This requirement is clearly not met in the system of Figure 2 in D1 if both stages are considered together to be a gate since, as explained above, the output value of the first output port (which corresponds to the "clock pattern out" port in D1) is independent of the data value at the input ("data in" port). As to document D2, this only discloses a non-linear gate, therefore Claims 1 and 11 are also novel over this disclosure.

With regard to inventive step, document D1 is considered as the closest prior art, since this discloses a system (Figure 2) which is suitable for

performing clock division and which uses a feedback path, thereby providing the most promising starting point for a skilled person wishing to arrive at the present invention. The objective problem to be solved is therefore to provide a simpler system for performing clock recovery. The system of D1 is concerned with demultiplexing data in the time domain. The clock recovery circuit is an essential feature of the system of document D1, since it allows the same clock or routing pattern to be applied to the control input of a gate regardless of the data present at the gate output. This feature allows time domain multiplexed data to be demultiplexed and routed to either one of the first or second output ports. Without this clock recovery stage the system would no longer be able to perform its stated function of routing or demultiplexing data, therefore the skilled person wishing to arrive at the present invention would have no reasons to connect the output of the gate directly to the control input of the same gate without using the clock recovery stage. Also a combination of the teachings of documents D1 and D2 would not result in the subject-matter of Claims 1 or 11, since neither document discloses a feedback path between the output and control input of the gate. Therefore these claims involve an inventive step.

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments (Article 123(2) EPC)*

The board is satisfied that the amendments in Claim 1 are fairly supported by the passages in the original application documents referred to by the appellant. The adaptation of the description is equally admissible.

3. *Article 84 EPC*

3.1 The board does not concur with the objection in the decision under appeal that the claims do not comply with the requirement of Article 84 EPC because the features of Claim 8 are not included in the independent claims. As convincingly reasoned by the appellant, the patent application discloses three alternative ways of configuring the clock division circuit defined in Claim 11 and used in Claim 1. On page 2, line 33 to page 4, line 3 a first alternative is disclosed, wherein the delay period equals one bit period ("the period between bits"); this is further disclosed on page 4, line 17 to page 5, line 4; and on page 7, line 22 to page 8, line 21. A second alternative, including an initial programming phase, is disclosed on page 3, lines 4 to 8; and on page 5, lines 5 to 28. The third alternative involves the use of a semiconductor optical amplifier (SOA) enabling the circuit to exhibit spontaneous clock division. This is disclosed on page 3, lines 9 to 14; and on page 5, line 29 to page 6, line 21.

3.2 Since it is not apparent from the patent application as filed that the use of an SOA would be compulsory for the first two alternative configurations, this feature cannot be considered as an essential feature of the

independent claims. Therefore in the opinion of the board the requirements of Article 84 EPC are met.

4. *Patentability*

4.1 Novelty

4.1.1 The objection of lack of novelty raised against the original independent claims had been based on the disclosures in document D1 and D2 using a broad interpretation of the original claim language. The subject-matter in the set of claims on which the decision was based had been restricted and the objection pertaining to lack of novelty had not been repeated in the decision. Indeed, as argued by the appellant, the routing device in document D1 comprises a gate and a further clock pattern recovery device, wherein the gate is not configured as defined in Claims 1 and 11. Document D2 discloses an all-optical Mach-Zehnder demultiplexer and also does not disclose this feedback. The other available documents are less relevant.

4.1.2 The subject-matter of Claims 1 and 11 is therefore novel.

4.2 Inventive step

4.2.1 The board concurs with the appellant that document D1 discloses the closest prior art. The objective problem addressed by the difference between the subject-matter of Claims 1 and 11 and the circuit disclosed in D1 may be seen in providing a simpler circuit for clock recovery.

4.2.2 The arguments provided by the appellant that it would not appear to be obvious to modify the circuit in Figure 2 of document D1 by removing the clock pattern recovery device appear persuasive, and in any case it is not clear whether and how the claimed feedback between the gate output and a gating pulse input should then function.

4.2.3 Therefore the subject-matter of Claim 1 is considered to involve an inventive step within the meaning of Article 56 EPC. This applies equally to Claim 11.

4.2.4 Claims 2 to 10 and Claims 12 to 18 are dependent of independent Claims 1 and 11 and therefore they also define patentable subject-matter.

5. For the above reasons, the board finds that the appellant's request meets the requirements of the EPC and that a patent can be granted on the basis thereof.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent on the basis of the following documents:

Claims: 1, 2 and 10 to 13 filed with the letter of 15 February 2005;
3 to 9 and 14 to 18 filed with the letter of 12 December 2002;

Description: pages 1 to 3 filed with the letter of 11 February 2005;
pages 4 to 12 of the published application;

Drawings: sheets 1/9 to 9/9 of the published application.

The Registrar: The Chairman:

P. Martorana A. Klein