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D E C I S I O N
of 15 October 2004

Case Number: T 1098/02 - 3.4.3

Application Number: 94303951.1

Publication Number: 0628992

IPC: H01L 21/306

Language of the proceedings: EN

Title of invention:
Method of making semiconductor wafers

Applicant:
SHIN-ETSU HANDOTAI COMPANY LIMITED

Opponent:
-

Headword:
Wafer polishing/SHIN-ETSU

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - auxiliary request (yes)"
"Claimed upper limit - not an arbitrary limit"

Decisions cited:
-

Catchword:
-

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Case Number: T 1098/02 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 15 October 2004

Appellant: SHIN-ETSU HANDOTAI COMPANY LIMITED
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Chiyoda-ku
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Representative: Pacitti, Paolo
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 8 March 2002 refusing European application No. 94303951.1 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: G. L. Eliasson
M. B. Günzel

Summary of Facts and Submissions

I. European patent No. 94 303 951.1 was refused in a decision of the examining division dated 8 March 2002 on the ground that the subject matter of claim 1 filed with the letter dated 30 November 1998 did not involve an inventive step having regard to the prior art documents

D1: Patent Abstracts of Japan vol. 14, no. 524 [E-1003], 16 November 1990 & JP-A-02 222144 (D1a); and

D2: Patent Abstracts of Japan vol. 11, no. 7 [E-469], 9 January 1987 & JP-A-61 182 233.

II. The appellant (applicant) lodged an appeal on 25 April 2002 paying the appeal fee the same day. A statement of the grounds of appeal was filed on 1 July 2002 together with an English translation of document D1a.

III. In a communication accompanying summons to oral proceedings the Board expressed the provisional opinion that the subject matter of claims 1 to 5 did not involve an inventive step having regard to the prior art as acknowledged in the application which is reflected in Section 1.4, "Silicon Shaping" in the text-book:

D5: S.M. Sze, "VLSI Technology, Second Edition" (McGraw-Hill, New York, 1988), pages 34 to 44).

IV. In response to the above communication, the appellant filed amended claims 1 to 5 on 4 September 2004 with the letter dated 2 September 2004.

V. At the oral proceedings held on 15 October 2004, the appellant requested that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

Main Request:
Claims 1 to 5 filed on 4 September 2004 with the letter dated 1 September 2004

Description and Drawings as filed

Auxiliary Request
Claims:
Nos. 1 to 4 of the auxiliary request filed during the oral proceedings

Description:
pages 1 to 7, 7a, 8 to 15 of the auxiliary request filed during the oral proceedings

Drawings:
Figures 1 to 7 as filed.

VI. Claim 1 according to the main request reads as follows:

"1. A method of making semiconductor wafers comprising, in sequence, the steps of:

(a) slicing a monocrystalline ingot pulled in a monocrystalline ingot puller to obtain disk-

shaped wafers each having a front surface and a back surface;

(b) chamfering the wafer periphery thereby preventing cracks in and chipping off of the sliced wafer;

(c) lapping the chamfered wafer to flatten said front and back surfaces;

(d) etching the lapped wafer using an alkaline etching solution thereby to remove work damage retained following lapping of the wafer;

(e) mirror-polishing the etched wafer across said front surface; and

(f) cleaning the polished wafer thereby to remove any residual polishing slurry and any other foreign substances on the wafer;

characterised in that:

subsequent to step (d) and prior to step (e), said back surface is partially polished thereby to partly remove surface irregularities formed on said back surface during said alkaline etching step (d)."

VII. Claim 1 according to the auxiliary request differs from claim 1 of the main request in that the characterising part reads as follows (amendments with respect to claim 1 of the main request have been emphasised):

"subsequent to step (d) and prior to step (e), said back surface is partially polished thereby to partly remove surface irregularities formed on said back surface during said alkaline etching step (d);
and in that

the stock removal on said back surface effected by said partial polishing is restricted under 3.0 ㎜ in depth."

VIII. The appellant presented essentially the following arguments in support of his requests:

(a) Document D1 which was considered the closest prior art in the decision under appeal is concerned with improving simultaneous double-side polishing, whereas document D5 and the present invention are both concerned with single-side polishing. Therefore, document D1 should not be considered as the closest prior art when assessing inventive step.

(b) The method of document D5 has the disadvantage that particles may chip off the back surface of the wafer due to the large surface roughness of the back surface.

The present invention solves the above problem by introducing a step of partially polishing the back surface before the front surface is mirror polished.

(c) Since document D1 addresses essentially the same problem as that of the present application and solves this problem using a simultaneous double-sided polishing technique, the skilled person faced with the above technical problem would altogether abandon the single-side polishing technique known from document D5 and replace it

with the double-sided polishing method as taught in document D1.

(d) Regarding the auxiliary request, document D5 teaches a stock removal of 25 μm for the front surface which is much higher than the claimed upper limit of 3.0 μm, and therefore, the skilled person would not consider such small stock removal to be appropriate.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.

2. *Amendments and Clarity*

Claim 1 according to the main request is the combination of claims 1 and 5 as filed and has been further amended for clarity. Claims 2 to 5 according to the main request correspond to claims 2 to 4 and 6 as filed, respectively.

With respect to the main request, claim 1 according to the auxiliary request further contains the feature of claim 5 as filed. Claims 2 to 4 according to the auxiliary request correspond to claims 2 to 4 as filed.

The Board is therefore satisfied that the claims according to both the main request and the auxiliary request meet the requirements of Articles 84 and 123(2) EPC.

3. *Inventive step - Main Request*

3.1 Document D1/D1a was considered the closest prior art in the decision under appeal. It discloses a method of producing a wafer, where after the wafers have been sliced, lapped, and etched in an alkaline etching solution, the front and back surfaces are polished simultaneously in a modified double-side polishing technique where the back surface is polished to a lesser degree than the mirror-polished front surface, so that the surfaces can be distinguished easily (cf. abstract). Thus, in addition to the step of partially polishing the back surface, document D1 discloses the steps (a), (c), (d) and (e) of the claimed method.

3.2 Document D5 discloses a method of making semiconductor wafers comprising the following steps:

(a) slicing the monocrystalline ingot to wafers (cf. page 35, penultimate paragraph);

(b) chamfering the edges (i.e. bevelling or contouring the edges) of the wafers (cf. page 38, first paragraph; Figure 25);

(c) lapping the front and back surfaces of the wafers (cf. page 37, last paragraph; Figure 24);

(d) wet etching the lapped wafer to remove damage (cf. pages 38 to 40);

(e) mirror-polishing the upper surface (cf. Figure 27); and

(f) cleaning the polished wafer (cf. page 43, two last sentences).

3.2.1 As to the type of etchant to be used in connection with the etching step (d), it is mentioned in document D5 that only alkaline etchants are suitable for wafers having a diameter larger than 75 mm (cf. chapter 1.4.2), a limit which was significantly exceeded by wafers typically used at the priority dated of the application in suit (June 1993) (cf. D5, Figure 29).

3.3 The method according to claim 1 thus differs from the method of document D5 in that

(e0) the back surface is partially polished subsequent to step (d) and prior to step (e) to partly remove surface irregularities formed on the back surface during the alkaline etching step (d).

3.4 As the appellant argued, document D1 is solely concerned with improving double-sided polishing, a technique where the front and back surfaces are polished simultaneously, whereas the method according to the application in suit relates to single-side polishing where only one surface at a time is polished (cf. item VIII(a) above). Therefore, the Board agrees with the appellant that although document D1 has many features in common with the method according to claim 1, it should not be considered closest prior art, since there would be no logical reason for treating document D1 as the starting point when assessing inventive step in the present case. Instead document D5, which corresponds to the prior art as described in the

application in suit (cf. application as published, column 1, line 10 to column 2, line 2), should be considered the closest prior art.

3.5 As described in the application in suit, the method such as disclosed in document D5 has the problem that particles might chip off the back surface due to the relatively large surface roughness of the back surface (cf. column 2, lines 3 to 8 and column 2, line 54 to column 3, line 9). The large surface roughness is caused by the alkaline etchant which has to be used in wet etching step (d) in order to preserve flatness of the wafer surfaces.

Although document D5 does not disclose the above problem, the appellant conceded at the oral proceedings that the problems caused by the increased surface roughness of the back surface were known in the art.

3.6 The appellant argued that a skilled person faced with the above technical problem would abandon the single-side polishing technique known from document D5 altogether and replace it with a double-sided polishing technique, such as that known from document D1, since double-sided polishing was known in the art as a solution to the problems caused by large surface-roughness of the back surface (cf. item VIII(c) above).

3.6.1 The Board finds however that the skilled person faced with the above problem with wafers produced according to the conventional method would immediately realize that this problem of chipping off of the particles can be solved by polishing the back surface at some convenient stage in the wafer processing. It would also

be clear to the skilled person that the back surface does not have to be perfectly mirror polished, since it was well-known in the art that wafers which underwent an acid etch treatment did not have to be polished at all on the back side. As mentioned above, the acid etch was however known to be unsuitable for large wafers for the reason of poor surface flatness (cf. D5, chapter 1.4.2).

3.6.2 Furthermore, the skilled person would also realize that it would only make sense to polish the back surface before the front surface is mirror-polished, since otherwise the mirror-polished front surface, which would be required to be held in contact with a wafer holder, would be damaged during the polishing of the back surface.

3.6.3 Therefore, although the skilled person would be aware of double-sided polishing techniques of the type known from document D1 where both surfaces are polished simultaneously, he would consider the sequential polishing of the back and front surfaces to be a suitable alternative for solving the technical problem of eliminating particles from chipping off the back surface, in particular since this alternative has the advantage that the existing equipment for single-sided polishing can be used. The solution suggested in document D1, on the other hand, requires a completely different apparatus from that disclosed in document D5 for polishing the wafers.

3.7 For the above reasons, the subject matter of claim 1 according to the main request does not involve an inventive step within the meaning of Article 56 EPC.

4. *Inventive step - Auxiliary Request*

4.1 With respect to the main request, claim 1 according to the first auxiliary request further specifies that in the step of partially polishing the back surface, the stock removal on the back surface effected by the partial polishing is restricted under 3.0 μm in depth.

4.2 As mentioned above in connection with the main request, the method described in document D5 does not include a step of polishing the back surface of a wafer. In the step of mirror-polishing the upper surface of a wafer, it is disclosed in document D5 that the typical stock removal on the front surface is about 25 μm of depth (cf. page 43, first paragraph).

4.3 According to the application in suit, the restriction of the stock removal to under 3.0 μm in depth represents the minimal amount that suppresses the generation of particles, and therefore minimizes the time taken by the step of polishing the back surface (cf. column 5, lines 40 to 48).

Furthermore, in order to be able distinguish the front and back surfaces, it is established in the application in suit that the glossiness of the back surface has to be at the most 98%. Figure 3 of the application in suit shows the glossiness of the back surface as a function of stock removal. It follows from Figure 3 that in order to limit the glossiness to under 98%, the stock removal should be restricted to be at most 3.0 μm (cf. column 5, columns 49 to 55).

Therefore, the restriction of 3.0 μm in depth on the stock removal on the back surface in the claimed method is not an arbitrary limit, but it represents the extent to which the back surface needs to be polished for suppressing the generation of particles, and at the same time, for allowing the front and back surfaces to be distinguishable from each other.

4.4 Therefore, in addition to avoiding particles from chipping off the back surface of the wafer, the method of claim 1 according to the auxiliary request further solves the problem of allowing the front and back surfaces of the wafer to be readily distinguishable.

4.5 It follows from the discussion above in respect of the main request that the Board is of the opinion that the skilled person faced with the problem of particles chipping of the back surface of wafers produced according to the method of document D5 would consider polishing the back surface before the front surface is polished. As convincingly argued by the appellant, however, the skilled person when deciding to what degree the back surface should be polished would use the typical stock removal value of 25 μm for polishing the front surface as a starting point for routine experiments (cf. item VIII(d) above). Since the claimed upper limit of 3.0 μm for the stock removal on the back surface is much smaller than what is typically removed from the front surface, the Board agrees with the appellant that the skilled person would not arrive at the claimed limit by routine experiments.

Therefore, in the Board's judgement, the subject matter of claim 1 according to the auxiliary request involves an inventive step within the meaning of Article 56 EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent with the following documents:

Claims:
Nos. 1 to 4 of the auxiliary request filed during the oral proceedings

Description:
pages 1 to 7, 7a, 8 to 15 of the auxiliary request filed during the oral proceedings

Drawings:
Figures 1 to 7 as filed.

The Registrar: The Chairman:

P. Cremona R. K. Shukla