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D E C I S I O N
of 25 November 2005

Case Number: T 0687/02 - 3.5.01

Application Number: 97120398.9

Publication Number: 0833506

IPC: H04N 7/01, G09G 1/16

Language of the proceedings: EN

Title of invention:
Memory system for use in an image date processing apparatus

Applicant:
FUJI PHOTO FILM CO., LTD.

Opponent:
-

Headword:
Memory system/FUJI PHOTO FILM

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0687/02 - 3.5.01

D E C I S I O N
of the Technical Board of Appeal 3.5.01
of 25 November 2005

Appellant: FUJI PHOTO FILM CO., LTD.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 15 February 2002 refusing European application No. 97120398.9 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: S. Steinbrener
Members: W. Chandler
G. Weiss

Summary of Facts and Submissions

I. This appeal is against the decision of the examining division to refuse the application on the ground that the subject-matter of claim 1 did not involve an inventive step (Article 56 EPC) having regard to the following documents:

D1: US-A-4 956 707

D2: Kohiyama K. et al.: "Development of a digital TV system for use in computer systems", IEEE Transactions on Consumer Electronics, vol. 35, no. 3, August 1989, NEW YORK US, pages 624-628

II. The appellant (applicant) lodged an appeal against the decision and paid the prescribed fee. The appellant requested that the decision under appeal be set aside and a patent granted, on the basis of the refused claims.

III. The appellant did not reply to the Board's communication accompanying the summons to oral proceedings. At the oral proceedings, the appellant requested that the decision under appeal be set aside and a patent granted based on the claims 1 to 5 filed during oral proceedings before the examining division on 5 February 2002.

At the end of the oral proceedings, the Chairman announced the decision.

IV. Claim 1 reads as follows:

"A memory system for use in an image data processing apparatus, comprising:
an image data memory (156) having a storage capacity of a frame of image data; and
programmable control means (142) for writing in and reading out image data to and from said image data memory;
characterized in that
said image data memory is provided in single (156) and adapted for selectively storing therein either one of natural image data and computer graphics data in the form of a frame of image data;
said programmable control means (142) using both interlaced and non-interlaced video data formats as read/write timing data formats for said image data memory (156) to cause either one of natural image data formats and computer graphics data formats to be written in and the other of the natural image data formats and computer graphics data formats be read out from said image data memory (156);
said programmable control means (142) being programmed in response to the image data and timing data so as to write in the image data to said image data memory (156) using write timing data corresponding to the timing data."

V. The appellant argued essentially as follows:

D1 was the closest prior art because it disclosed a memory system for converting from computer graphics format to natural image (television) format. It also had programmable control means because the user could

interactively adjust the front panel controls while observing the converted image on a monitor. However, it did not disclose a conversion in the other direction.

D2 disclosed a memory system for converting from television format to graphics format, but with no programmable control means.

The invention was more than a simple combination of the individual conversions of D1 and D2 into a single device. Firstly, both conversions made use of a single memory block. Secondly, the invention used a common programmable control means to control the memory. Finally, the particular conversions in D1 and D2 were such that it was not possible to use a common memory and a common control means without modifications. Specifically, in the frame memory of D1, the preceding horizontal filters had already reduced the number of samples. In D2, the frame memory stored only the final signal after conversion in the preceding clock rate conversion circuits including horizontal and vertical filters and interpolation circuits, and was essentially only a display memory. The invention had only a single memory controlled by a programmable controller that performed all of the bi-directional conversion operations.

Apart from the fact that there was no hint to provide both conversions in a single apparatus with a common memory and a programmable control means, the invention also solved the problem of actually enabling the use of a common memory. Although this resulted in a simplification of the existing circuits so that they

could be combined, such simplifications were often only apparent with hindsight.

Reasons for the Decision

1. The appeal complies with the requirements referred to in Rule 65(1) EPC and is, therefore, admissible.

2. The application states, at column 5, lines 1 to 5, that the object of the invention is to provide a memory system capable of handling (meaning in particular converting between them – see lines 21 to 26) a variety of image signal formats using a minimum amount of hardware.

3. It is common ground that D1 discloses a memory system with an image data memory for storing computer graphics (e.g. VGA) data and control means providing signals for converting it to natural image (e.g. television) data. Similarly, D2 discloses the same for a conversion in the other direction.

4. The Board however judges that D2 is in fact closer prior art than D1. This is because D2 also mentions at page 627, right-hand column, under point (1) of the advantages that a "single memory block is used economically" for scan rate conversion, namely the above-mentioned object of the invention.

5. At the oral proceedings, the appellant gave less emphasis than in the preceding phase of the proceedings to the claimed characteristics of the memory having a storage capacity of a frame of image data and being

provided "in single". Nevertheless, the Board judges that it is implicit from the fact that the above-mentioned paragraph in D2 mentions that the memory is used for picture freeze that it must have at least this storage capacity, and, hence, falls under the claimed capacity. Secondly, even if the expression "in single" implies any technical limitation, it is also disclosed in the above-mentioned paragraph.

6. The appellant argued that in D2, the frame memory was not part of the conversion process, but was essentially only a display memory. However, the Board cannot agree with this because D2 states, for example, at page 627, right-hand column, third paragraph, that:

"To convert the horizontal and vertical scan rates for TV pictures into those for computer systems, the memory control LSI writes input TV signals into memory at the TV scan rate and reads the written signals at computer scan rates. …"

It is clear from this passage that the memory is part of the conversion, at least, of the scan rates.

7. Moreover, the above-quoted passage shows that D2 discloses the following features of claim 1:
storing natural image data (TV signals);
control means using interlaced video data formats (TV signals) as write timing data formats for said image data memory to cause natural image data format (TV signals) to be written in and computer graphics data format be read out from said image data memory;
said control means responsive to the image data and timing data so as to write in the image data to said

image data memory using write timing data corresponding to the timing data.

8. Thus, the Board judges that claim 1 differs from D2 in that the memory stores computer graphics data in addition to natural image data (part of the first feature of the characterising portion), and that it has programmable control means (part of the second feature of the preamble) providing memory timing signals to write computer graphics data and to read natural image data (part of the second and third features of the characterising portion) in addition to the other way around.

9. The Board judges that the above-mentioned differences solve the problem of providing a more flexible apparatus.

10. The Board judges that it would indeed be an obvious possibility to consider this general problem and solve it by providing a memory system that converts both ways. Firstly, a conversion in the reverse direction is already known, from D1, for example. Secondly, D2 describes the desirability of making TV systems "compatible" with other digital systems (abstract, lines 8 to 10), and "merging and integrating computer and TV images" (page 624, "Background", lines 1 to 2). D2 describes the conversion from TV images to computer images because computers are suited to image processing and television is an inexpensive source of image information (see page 624, under "Background", second to fourth paragraphs). However, the Board judges that it is an obvious possibility when integrating computer and TV images to consider also using other capabilities

of television equipment, such as using video tape recorders as an inexpensive source of image storage, and thus to consider converting computer images to TV format.

11. In order to modify the memory system of D2 to convert in the other direction, the Board judges that firstly it is obvious, e.g. from D1, to use a frame memory and perform the converse read and write operations. Secondly, an electronic circuit designer is always considering the possibility of reusing common circuitry. Thus it is obvious to consider the general idea of using the same memory for the converse conversion, rather than providing a second frame memory. This is all the more so in this case since a memory that can store a complete frame, such as that in D2, is an expensive part of the circuit, especially at the priority date of the application. Regardless of the memory configuration, it is evident that the control means must provide corresponding converse read and write timing signals as claimed. Finally, the Board judges that the use of a programmable control means as opposed to, say, dedicated control circuitry is a matter of routine circuit design, and depends on the desired degree of flexibility of the operating parameters of the circuit.

12. The appellant argued that it was not possible to combine the particular conversions of D1 and D2 to use a single memory without modifications. Firstly, however, the Board notes that the conversions actually claimed in claim 1, and consequently the teachings that need to be combined, are merely defined in functional terms. Thus, the appellant's argument can at most mean that D1

and D2 teach away from the idea itself, but not any particular implementation of it. However, the Board judges that it is common knowledge in this field, or at least derivable from D2 at page 626, last two paragraphs to page 627, first paragraph that the basic format conversions can be achieved by simply reading in and out the correct number of samples at the correct rate. Interpolation or filtering is preferable to reduce aliasing error, but not strictly required. The Board thus judges that the skilled person would not be led away from the claimed basic idea by the additional filters disclosed in D1 and D2, but would realise that they are specific implementations of improvements that may also be required in some form in the claimed system.

13. The Board judges that claim 1 accordingly does not involve an inventive step (Article 56 EPC).

14. Since there are no other requests, it follows that the appeal must be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Kiehl S. Steinbrener