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D E C I S I O N
of 3 December 2004

Case Number: T 0613/02 - 3.5.2

Application Number: 96938370.2

Publication Number: 0875092

IPC: H03K 3/037

Language of the proceedings: EN

Title of invention:
Logic circuits

Applicant:
MBDA UK Limited

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56, 123(2)

Keyword:
"Admissibility of the amendments (yes)"
"Inventive step - after amendment (yes)"

Decisions cited:
G 0001/92

Catchword:
-

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Case Number: T 0613/02 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 3 December 2004

Appellant: MBDA UK Limited
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Representative: Jewess, Michael
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 23 November 2001 refusing European application No. 96938370.2 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: J.-M. Cannard
C. Holtz

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division to refuse European patent application No. 96 938 370.2. The reason given for the refusal was that the subject-matter of claim 1 did not involve an inventive step within the meaning of Article 56 EPC having regard to the prior art document D1: DE-A-3 813 816.

II. The documents:

D1: DE-A-3 813 816, cited in the Search Report, and

the prior art acknowledged in the application (see published application WO97/18629) with reference to figure 1,

are relevant to the present appeal.

III. The current version of claim 1, filed with the letter dated 16 June 2004, reads as follows:

"A transparent latch comprising four logic gates (5, 6, 7 and 8) in which,

a first input to the second gate (6) is arranged to receive a signal input (D),

an input to the first gate (5) is arranged to receive a control input (C) to determine whether the latch will be in a first operating mode in which the logic state of the signal input (D) will propagate to an output (Q), or in a second operating mode in which any logic level change in the signal input (D) will be blocked from reaching the output (Q),

an output from the second gate (6) and an output from the third gate (7) are connected to respective inputs to the fourth gate (8),

and the output (Q) from the fourth gate (8) is connected to a first input to the third gate (7),

characterised in that the output (Y) from the second gate (6) is connected to another input to the first gate (5), an output from the first gate (5) is connected to a second input to the second gate (6), and the control input (C) is connected to an input of the third gate (7)."

Claims 2 to 5 are dependent on claim 1.

IV. The arguments of the appellant can be summarized as follows:

Claim 1 set out a structural difference over the prior art known from document D1. In the transparent latch according to claim 1, the circuit output (A) was taken from the output of that one of the second pair of gates which received the output signal from the first pair of gates. In D1 the circuit output (A) was taken from the output of that one of the second pair of gates which received the clock signal (E). D1 taught a circuit for enabling or disabling a timing signal according to a gating signal, without having to change the timing pulse width, and was recommended for use as a gate for measuring the frequency of a timing signal. The circuit of D1 was not a latch, or a transparent latch, and performed a totally different function to the circuit according to claim 1. It was not obvious to modify the circuit of D1 to turn it into a latch or to realise a different function by taking the output from a

different gate. The skilled person seeking to address the problem of incorrect latching due to propagation delays in latches would not have considered D1 to be relevant to his problem.

V. The appellant requested that the decision under appeal be set aside and that a patent be granted in the following version:

claims: 1 and 2 filed with letter of 16 June 2004; claims 3 to 5 filed with letter of 29 September 2004;

description: pages 1, 3, 5 to 8 filed with letter of 16 June 2004; pages 2 and 4 filed with letter of 29 September 2004;

drawings: as originally filed.

Reasons for the Decision

1. The appeal is admissible.

Amendments

2. The Board is satisfied that the claims and description according to the present request meet the requirements of Article 84 EPC and do not contravene Article 123(2) EPC.

2.1 This applies in particular to present claim 1 which relates to a transparent latch having a signal input (D), an operating mode control input (C), an output (Q),

and including logic gate means for allowing the output signal (Q) to follow the input signal level (D) in a first operating mode, and for blocking any level change in the signal input (D) from propagating through to the output (Q) in a second operating mode, as this appears from claim 1 and the description (published application WO97/18629, page 3, lines 14 to 20) as filed. According to the specific embodiment described on page 4, lines 8 to 14 of the description, the latch consists of two pairs of logic gates in which the output of each gate comprising a pair is fed back to the input of the other gate comprising the same pair, the control input (C) is applied to both pairs with the signal input (D) being applied just to a first pair, and the output of the first pair is connected to an input of the second pair. According to the only example of realisation described in the application as filed, with reference to figure 2, the output of that one of the gates of the first pair of gates which does not receive the control input (C) is connected to an input of that one of the gates of the second pair of gates whose output forms the latch output (Q). Therefore, the latch according to claim 1 does not extend beyond the content of the original application.

2.2 Dependent claims 2 and 3 to 5 are respectively supported by dependent claim 4 and the description on page 5 of the application as filed.

Novelty and inventive step

3. The novelty of the subject-matter of claim 1 has not been disputed and it is novel. Neither the prior art acknowledged in the application (see figure 1 and

related description), nor any one of the cited prior art documents discloses a latch which comprises a first and a second pair of logic gates in which the output of each gate is fed back to the input of the other gate, and the output of the gate not receiving a control signal in the second pair forms the latch output, as recited in claim 1.

4. Claim 1 is correctly delimited against the prior art circuit acknowledged in the description with reference to figure 1, which forms the closest prior art. Starting from this prior art, and having regard to the technical effects achieved by the invention (see the application as published, pages 2 and 3, the bridging paragraph), the objective problem addressed by the invention could be seen as providing a transparent latch in which propagation delays through gates and interconnecting wires could not affect the proper operation of the latch. This problem is solved by the transparent latch according to claim 1.

5. A suggestion of the claimed invention cannot be found in the prior art acknowledged in the application (which differs from the latch according to claim 1 by the three independent features recited in the characterizing part), nor in any of the prior art documents cited in the Search Report, taken alone or in combination.

5.1 This applies in particular to D1. The Board does not share the examining division's view according to which D1 (figure 3) discloses a latch in which an input signal applied on the (M) input propagates through to

the output of gate 3, or is blocked according to the state of a control signal applied on the (E) input.

5.1.1 The circuit according to figure 3 of D1 is a gating circuit for enabling or disabling a clock signal (E) according to the state of a gating signal (M). This circuit, which differs from the latch according to claim 1 in that its circuit output is taken from the output of that one of the gates of the second pair of gates which receives the control signal, does not perform the function of a transparent latch for propagating or blocking a logical state of an input signal (M), applied to a first gate of a first pair of gates, according to the state of a control signal (E) applied to a gate of the first and second pair of gates.

5.1.2 The skilled person, faced with the problem of improving latches, might however consider starting from the circuit of D1 because, according to figures 4 and 5 of D1, the logic state of the clock signal (E) propagates through to the output, or is blocked, according to a first and a second operating mode dependent upon the logic state of a gating signal (M).

5.1.3 But, there is no disclosure in D1 of applying a control signal on the (E) input and an input signal, to be propagated or blocked, on the (M) input, as in the latch according to claim 1, and the characteristics of the circuit of D1 revealed by such a use, in particular a "latched" signal at the output of gate 3, are extrinsic characteristics, which cannot be considered as having been made available to the public (G 1/92 OJ EPO 1993, 277, reasons 1.2 and 3). Nor is it obvious to consider the signal on the (E) input as a control

signal and the signal on the (M) input as an input signal to be transmitted to the output of gate 3, because this view would be in contradiction with the teaching of D1 as a whole. Accordingly, there is no obvious reason for the skilled person to modify the circuit of D1 by taking the output of gate 3 (the gate not receiving the control signal in the second pair) as the circuit output.

5.2 D1 mentions neither a problem caused by propagation delays through gates and wires, nor a solution to the problem addressed by the invention. Therefore there is no reason for the skilled man to consider combining the prior art acknowledged in the application with the teaching of D1.

6. For the foregoing reasons, in the Board's judgement the subject-matter of claim 1 according to the present request is considered to be new and to involve an inventive step within the meaning of Articles 54 and 56 EPC. The application as amended meets the requirements of the EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

claims: 1 and 2 filed with letter of 16 June 2004; claims 3 to 5 filed with letter of 29 September 2004;

description: pages 1, 3, 5 to 8 filed with letter of 16 June 2004; pages 2 and 4 filed with letter of 29 September 2004;

drawings: as originally filed.

The Registrar: The Chairman:

D. Sauter W. J. L. Wheeler