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D E C I S I O N
of 20 July 2004

Case Number: T 0594/02 - 3.5.2

Application Number: 99304467.6

Publication Number: 0967726

IPC: H03M 1/08

Language of the proceedings: EN

Title of invention:
Method and apparatus for extending the spurious free dynamic range of a digital-to-analog converter

Applicant:
LUCENT TECHNOLOGIES INC.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 54(1), 56

Keyword:
"Novelty (yes)"
"Inventive step (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0594/02 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 20 July 2004

Appellant: Lucent Technologies Inc.
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Representative: Williams, David John
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 23 October 2001 refusing European application No. 99304467.6 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: M. Ruggiu
C. Holtz

Summary of Facts and Submissions

I. The applicant filed an appeal against the decision of the examining division to refuse European patent application Nr. 99 304 467.6.

II. The reason given for the refusal was that the subject-matter of the independent claims 1 and 6 was not new.

III. The decision under appeal cited the following prior art document:

D1: JP-A-03 089 627.

The PAJ abstract (in English) of D1 has been published in 1991 and is itself part of the state of the art.

The appellant indicated in a letter dated 21 June 2004 that a full translation of D1 was available to him. He did not file this translation, although he was invited to do so in a communication of the board.

IV. Oral proceeding took place before the board on 20 July 2004. As announced in a letter of 19 July 2004, the appellant was not represented at the oral proceedings.

It was noted that the appellant requested that the decision under appeal be set aside and that a patent be granted in the following version:

Description

Pages 2a, 5 and 11 filed with letter of 19 July 2004,
Page 2 filed with letter of 21 June 2004, and
Pages 1, 3, 4, 6 to 10, 12 and 13 of the application as filed.

Claims

No. 1 to 9 filed with letter of 19 July 2004,

Drawings

Sheets 1/6 to 6/6 of the application as filed.

V. Claim 1 reads as follows:

"A method of converting a digital input signal (S) to analog form, said digital input signal (S) having an amplitude defined by N bits, the method comprising the steps of:
adjusting the amplitude of the digital input signal (S) to obtain an adjusted signal (S + D) on a first path (16) and a distortion signal (D*) on a second path (18);
converting the adjusted signal (S + D) on the first path (16) to analog form by a first analog to digital converter (12) to produce a first analog signal (S' + D');
converting the distortion signal (D*) on the second path (18) to analog form by a second analog to digital converter (14) to produce a second analog signal (D*');
combining said first analog signal (S' + D') and said second analog signal (D*') to produce a converted analog signal (S) [sic] with a lower amplitude of spurious distortion when compared to the amplitude of spurious distortion if the digital input signal (S) had been converted by the first digital to analog converter

(12);
said method CHARACTERISED BY:
routing the n2 most significant bits of said digital input signal (S) onto said first path (16) as said adjusted signal (S + D), thereby clipping the amplitude of the digital input signal (S); and
routing the remaining n1 least significant bits of the digital input signal (S) onto said second path (18) as said distortion signal (D*)."

Claim 6 reads as follows:

"A digital to analog converter system for converting a digital input signal (S) to a converted analog signal (S'), said digital input signal having an amplitude defined by N bits, said system comprising:
means for adjusting the amplitude of the digital input signal (S) to obtain an adjusted signal (S + D) on a first path (16) and a distortion signal (D*) on a second path (18);
a first analog to digital converter (12) for converting the adjusted signal (S + D) on the first path (16) to analog form and to thereby produce a first analog signal (S’ + D’);
a second analog to digital converter (14) for converting the distortion signal (D*) on the second path (18) to analog form and to thereby produce a second analog signal (D*’);
a combiner (20) coupled to said first and second paths operative to combine said first analog signal (S’ + D’) and said second analog signal (D*’) to produce a converted analog signal (S) [sic] with a lower amplitude of spurious distortion when compared to the amplitude of spurious distortion if the digital input

signal (S) had been converted by the first digital to analog converter (12);
said system CHARACTERISED IN THAT:
the n2 most significant bits of said digital input signal (S) are routed onto said first path (16) as said adjusted signal (S + D), thereby clipping the amplitude of the digital input signal (S), and
the remaining n1 least significant bits of the digital input signal (S) are routed onto said second path (18) as said distortion signal (D*)."

Claims 2 to 5 are dependent on claim 1 and claims 7 to 9 on claim 6.

VI. The appellant argued essentially as follows:

Reference D1 disclosed a digital/analog converter (DAC) system including dual DAC units and concerned an application where a voltage shift signal was added to the input signal to address certain known problems of input signals at the point of crossing zero volts. Because of the addition of the DC bias to the input signal, the input of the DAC could exceed the dynamic range of the DAC itself, thus generating large waveform distortion. Figure 1 of D1 showed a system in which a shift signal generation circuit 2 generated a shift signal B that was added to the digital input signal A by a digital adder 3 to generate C = A + B. A level detection circuit 4 determined whether the adder output C reached a predetermined level that had been set at or below overflow of a first DAC 5. A digital limiter 6 connected to the adder 3 and to the level detection circuit 4 outputted the adder output C unchanged if it did not reach the predetermined level. If the adder

output C was at or above the predetermined level, the digital limiter 6 continuously outputted a digital value at a given level. A digital subtraction circuit 7 having one input connected to the adder 3 and another input connected to the limiter 6 provided a compensation signal E = C - D. The compensation signal E was equivalent to a component which had been cut off by the limiter 6. A digital subtractor 8 was connected to the shift signal generation circuit 2 and the subtraction circuit 7 and outputted a signal F = B - E. The first DAC 5, which had a dynamic range that was the same as that of the adder 3, converted the output D of the limiter 6 to an analog signal. A second DAC 9 converted the output F of the subtractor 8 to an analog signal. Finally, an analog subtraction circuit 10 subtracted the output of the second DAC 9 from the output of the first DAC 5 to obtain the output waveform. While the periodic removal of a DC bias from an input signal might literally have constituted a reduction in amplitude, it was clear that such a removal of a constant DC offset had no effect on the operational amplitude of the input signal itself. Furthermore, the distortion addressed by D1 was an internal distortion of the DAC occurring from the DC bias of the input signal causing that signal to exceed the dynamic range of the DAC.

The only similarity between D1 and the invention was that both employed dual DAC units arranged to operate on separate portions of an input digital signal. However, there was no similarity at all between the approach of D1 and that of the invention for determining the input parameters for the respective DAC units. In contrast to the complex arrangement of D1,

the invention achieved its goal of improving the spurious free dynamic range (SFDR) of the DAC system by simply dividing the digital input signal into two parts, a first part comprising the n2 most significant bits (MSB) of an N bit input word and a second part comprising the remaining n1 least significant bits (LSB) (N = n2 + n1). The n2 bits of the first part, representing the input signal S plus a distortion component D, were routed onto a first path towards a first DAC. The n1 bits of the second part, representing an amount of amplitude clipping for the input signal and designated distortion D*, were routed via a second path to a second DAC. After operation by the respective DAC units on the first and second paths, the analog outputs thereof were recombined to form the analog output of the DAC system corresponding to the digital input of that system. The amplitudes of the signals S + D and D* were reduced with respect to the amplitude of the digital input signal S, so that the D/A conversion was performed on lower amplitude signals on the separate paths before recombining the signals. The DAC system of the invention thereby produced the desired converted analog signal S' with an improved SFDR. The spurious distortion which was addressed by the invention was different from the internal DAC distortion addressed by D1. Furthermore, the way in which the present invention reduced spurious distortion was clearly different from the way the system of D1 operated.

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments*

2.1 In the application as filed the reference S' designates the converted analog signal. It is therefore immediately apparent that the reference "(S)" must be amended to read "(S')" where it follows the expression "converted analog signal" in claim 1 (line 17 of page 14) and in claim 6 (line 1 of page 16).

2.2 The last paragraph of page 2 of the description filed with the letter of 21 June 2004 indicates that "according to a further aspect of the present invention, there is provided a digital to analog converter system ... as defined in claim 7". Following the amendments to the claims filed with the letter of 19 July 2004, claim 6 is now the independent claim directed to the digital to analog converter system. It is therefore immediately apparent that the expression "claim 7", which appears in the last line of page 2 of the description, must be amended to read "claim 6".

2.3 The application as originally filed included method claims (claims 1 to 8 and 15) and apparatus claims (claims 9 to 14 and 16). The features of present claims 1 and 6 can be found in claims 9 to 11 as originally filed. Regarding present claims 2 and 7, the feature that a summer combines the analog output (S' + D') from the first DAC with the analog output (D*') from the second DAC is described on page 6, lines 13 to 15, of the description as originally filed.

The feature of present claim 3 corresponds to the one specified in claim 4 as originally filed. The feature of present claim 8 can be found in claim 12 as originally filed. The features of present claims 4 and 9 can be found on page 10, lines 11 to 20, of the description as originally filed. The feature of present claim 5 corresponds to the one specified in claim 8 as originally filed.

2.4 The description has been amended to cite document D1 and indicate the background art disclosed therein. Furthermore, the description has been amended to make it consistent with the claims and to correct a clerical error on page 11.

2.5 Thus, the application has not been amended in such a way that it contains subject-matter which extends beyond the content of the application as filed. Therefore, the amendments do not contravene Article 123(2) EPC.

3. *Novelty*

4. It is not contested that D1 discloses a system and a corresponding method for converting a digital input signal to analog form. As is generally known, the digital input signal of D1 must have its amplitude defined by a certain number N of bits. In D1, the digital input signal A is digitally manipulated by components 2, 3, 4 and 6 to obtain a digital signal D having a changed amplitude on a first path connected to the input of a first digital to analog converter (DAC) 5. In the view of the board, the manipulation of the digital input signal to change its amplitude performed

in the system of D1 falls within the terms used in claims 1 and 6 of the present application ("adjusting the amplitude of the digital input signal to obtain an adjusted signal"). A further signal F = D - A is obtained in the system of D1, by means of components 7 and 8, on a second path connected to the input of a second DAC 9. A subtracting circuit 10 subtracts the analog output of the second DAC 9 from the analog output of the first DAC 5 and thereby produces a converted analog signal corresponding to the digital input signal A. In the view of the board, a subtraction of analog signals as performed by the circuit 10 of D1 can be regarded as a combination of signals. The PAJ abstract of D1 further states that the purpose of the system described there is to obtain an analog signal with less distortion. Thus, the board considers that the features specified in the pre-characterising portions of claims 1 and 6 of the present application are part of the prior art disclosed in D1, in particular in its PAJ abstract.

4.1 The manipulation of the digital signal in D1 involves in particular adding a shift signal B to the digital input signal A. It is therefore apparent that this digital manipulation does not result in routing the n2 most significant bits of the digital input signal on the first path to the input of the first DAC 5. This also implies that the signal F, which in the system of D1 is applied to the input of the second DAC 9 and represents the difference between the signal D applied to the input of the first DAC 5 and the digital input signal A, cannot correspond to the n1 least significant bits of the digital input signal.

The features of the characterising portions of claims 1 and 6 of the present application are therefore not part of the prior art disclosed in D1.

4.2 Thus, the subject-matter defined by claims 1 and 6 is considered to be new in the sense of Article 54(1) EPC. Furthermore, the board considers that claims 1 and 6 are properly cast in the two-part form specified in Rule 29(1) EPC.

5. *Inventive step*

According to the present application, a lower amplitude of spurious distortion can be obtained by routing the n2 most significant bits of a digital input signal A on a first path to the input of a first DAC and the remaining n1 less significant bits on a second path to the input of a second DAC and combining the analog outputs of the two DACs. Such a teaching is completely incompatible with the prior art system described in D1. Nothing in D1 or in the only other document cited in the European search report (which relates to analog to digital conversion and not digital to analog conversion as the present application and D1) suggests this feature. The board considers therefore that, having regard to the state of the art, this feature is not obvious to a person skilled in the art. Thus, the subject-matter of claims 1 and 6 is considered to involve an inventive step in the sense of Article 56 EPC.

6. The subject-matter of claims 2 to 5 and 7 to 9, which are dependent on claims 1 and 6, is thereby also considered as being new and involving an inventive step.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent in the version requested by the appellant, namely:

Description
Pages 2a, 5 and 11 filed with letter of 19 July 2004,
Page 2 filed with letter of 21 June 2004, and
Pages 1, 3, 4, 6 to 10, 12 and 13 of the application as filed,

Claims
No. 1 to 9 filed with letter of 19 July 2004,

Drawings
Sheets 1/6 to 6/6 of the application as filed,

with the correction of three obvious clerical errors, namely: in claim 1, line 17, "signal (S)" to read "signal (S')", in claim 6, line 1 of page 16, "signal (S)" to read "signal (S')", and in the last line on page 2 of the description, "claim 7" to read "claim 6".

The Registrar: The Chairman:

D. Sauter W. J. L. Wheeler