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D E C I S I O N
of 25 March 2004

Case Number: T 0423/02 - 3.5.2

Application Number: 98305988.2

Publication Number: 0896430

IPC: H03K 3/356

Language of the proceedings: EN

Title of invention:
High-speed clock-enabled latch circuit

Applicant:
LUCENT TECHNOLOGIES INC.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 54, 56

Keyword:
"Novelty and inventive step (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0423/02 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 25 March 2004

Appellant: LUCENT TECHNOLOGIES INC.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 24 January 2002 refusing European application No. 98305988.2 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: J.-M. Cannard
C. Holtz

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division to refuse European patent application No. 98 305 988.2. On 25 January 2001, the examining division had issued a communication under Rule 51(4) EPC. In a letter dated 25 May 2001, the applicant expressed disapproval of the text proposed for claim 1 and page 23 of the description, and filed an amended sheet of claims 1 to 5 and an amended page 23. The examining division then refused the application. The reason given for the refusal was that the subject-matter of claim 1 filed with the letter dated 25 May 2001 did not meet the requirements of Articles 52(1) and 54(1) and (2) EPC, having regard to the prior art known from document D4: US-A-5 355 391.

II. The following documents:

D1: US-A-4 716 320,

D2: US-A-4 506 167,

D3: US-A-4 123 799,

considered in the first instance, and the other prior art documents cited in the search report:

D5: IBM Technical Disclosure Bulletin, vol. 32, no. 2, July 1989, pages 251 to 254,

D6: IBM Technical Disclosure Bulletin, vol. 29, no. 5, October 1986, pages 2160 to 2161, and

D7: WO-A-96/10866,

are also considered in this decision.

III. The current version of independent claim 1, which corresponds to claim 1 refused by the examining division, reads as follows:

Claim 1:

"A latch circuit (100) comprising:

first and second transistors (105, 110) coupled to each other at a first junction (115) and in series between a first voltage source (V_{DD}) and a controllable enable switch (120) coupled to a second voltage source (V_{SS}), a gate (112) of said second transistor being coupled to a first controllable input switch (140) receiving a first input signal;

third and fourth transistors (125, 130) coupled to each other at a second junction (135) and in series between the first voltage source and the controllable enable switch, a gate (132) of said fourth transistor being coupled to a second controllable input switch (145) receiving a corresponding second input signal, gates (107, 127) of said first and third transistors being coupled to said second and first junctions, respectively; and

a controllable initialization switch (150) coupled between the first and second junctions;

CHARACTERISED IN THAT the switches are controllable by a clock signal, wherein when the clock signal is at a first signal level, said controllable enable switch electrically connects the second and fourth transistors to the second voltage source, and when the clock signal is at a second signal level, the first and second controllable input switches provide the input signals to the gates of the second and fourth transistors and the controllable initialization switch electrically connects the first and second junctions."

Claims 2 to 13 are dependent on claim 1.

IV. The arguments of the appellant can be summarized as follows:

The term "junction", as utilised in the application, referred to a common circuit node and was not met by coupling via an active transistor whose state was a function of a clock signal. In the latch circuit disclosed in document D4, the transistors M13 and M3, which were coupled via a transistor M5, were connected to each other only when this transistor was rendered conductive by a clock signal, and the transistors M14 and M4, which were coupled via a transistor M6, were connected to each other only when this transistor was rendered conductive by the clock signal. The first and second junctions according to claim 1 were not disclosed in D4.

V. The appellant requested that the decision under appeal be set aside and that a patent be granted in the following version:

claims 1 to 5 and page 23 of the description, filed with the letter dated 25 May 2001; and claims 6 to 13, pages 1 to 22 of the description and Figures 1 to 6 of the drawings as attached to the communication under Rule 51(4) EPC dated 25 January 2001.

Reasons for the Decision

1. The appeal is admissible.

2. The Board is satisfied that claims 1 to 13 and the amendments to the description according to the present request meet the requirements of Article 84 EPC and do not contravene Article 123(2) EPC.

Novelty

3. The subject-matter of claim 1 is considered to be novel because none of the cited prior art documents discloses a latch circuit according to claim 1.

3.1 The latch circuit according to claim 1 comprises a first and a second transistor (105, 110) which "are coupled to each other at a first junction (115)", a gate of a third transistor (125) and a controllable initialization switch (150) being also coupled to this junction. According to the description with reference to Figures 2 and 3 (published application, paragraphs [0019] and [0024], a "first junction" is formed by a common circuit node (115) which is connected to a first and a second transistor, a controllable initialization switch, and the gate of a third transistor (105, 110, 150, 125). The first junction referred to in claim 1

thus should be understood as specifying a first common circuit node at which the circuit components referred to above are electrically coupled to each other, but cannot be so broadly construed as covering a connection via a component which is controllable to be conductive or non-conductive (such as transistor M5 in Figure 4b of D4), because such an interpretation is not supported by the application as a whole. The same conclusion applies to the "second junction" (135) recited in claim 1, at which a third and a fourth transistor (125, 130), the gate of the first transistor and the initialization switch are coupled to each other.

3.2 In the latch circuit according to D4 (column 6, lines 17 to 62; Figure 4b), a first transistor (M13) and the gate of a third transistor (M14) on the one hand, and a second transistor (M3) and a controllable switch (M7) on the other hand are coupled through an isolation transistor (M5) which is controlled to be conductive or non-conductive. Similarly, the third transistor (M14) and the gate of the first transistor (M13) on the one hand, and a fourth transistor (M4) and the controllable switch (M7) on the other hand are coupled through an isolation transistor (M6) which is controlled to be conductive or non-conductive. Accordingly, a first and a second junction with the meaning they have in claim 1 are not disclosed in D4 and the subject-matter of claim 1 is novel with respect to the disclosure of D4.

3.3 The wording of the characterizing part of claim 1 implies a structure of the latch circuit such that the first and second controllable input switches and the controllable initialization switch on the one hand, and

the controllable enable switch on the other one are controlled by a clock signal to operate in an opposite or complementary manner. None of the documents D1 to D3, and D5 to D7 discloses a latch circuit having such a feature.

Inventive step

4. Starting from D4, the objective problem addressed by the invention could be seen as providing a simpler latch circuit. However, the skilled person would not consider removing the isolation transistors (M5, M6) of D4 to get a first and a second junction in the form of respective common circuit nodes as specified in claim 1, because the latch circuit of D4 would not then work properly.

4.1 In the circuit of D4, when the clock is low, the controllable enabling switch (transistor M1) is off and the controllable initialization switch (transistor M7) is on, to equilibrate the drain nodes of transistors M3 and M4. At the same time, the isolation transistors (M5 and M6) are off to isolate the differential amplifier of the first stage consisting of transistors M1 to M4 from the differential amplifier of the second stage consisting of transistors M10 to M16, and power is supplied by the transistor M10, which is on, to activate the differential amplifier of the second stage. The drains and gates of the transistors M13 and M14 are isolated from each other by the transistor M16 which is off and the differential voltage is amplified. Moreover, "as the second stage is isolated from the first stage when the isolation transistors are turned off, large swing voltage levels are not back injected into the

DATA and V_{REF} inputs" (column 6, lines 48 to 51). Would the isolation transistors M5 and M6 be replaced by circuit nodes, the second stage would no longer be isolated from the first stage when the clock is low. Accordingly, the latch circuit would not work properly, firstly because the drains and gates of the transistors M13 and M14 would be short circuited by the transistor M7, so that the differential voltage of the amplifier of the second stage could not be developed, and secondly because large swing voltage levels could not be prevented from being back injected into the DATA and V_{REF} inputs.

5. Documents D1, D3, D5 and D6 relate to latching sense amplifiers for reading and writing data in a memory cell. There is no good reason for the skilled person to control the switches of the sense amplifiers disclosed in these documents by clock signals in the same way as the switches according to D4 are controlled. D2 and D7 relate to latch circuits without any controllable initialization switch connected between a first and a second junction respectively coupled to the first and second input transistors of the circuit, and thus are less relevant.

6. For the foregoing reasons, in the Board's judgement, the subject-matter of claim 1 and dependent claims 2 to 13 according to the present request is considered to be new and involve an inventive step within the meaning of Articles 54 and 56 EPC. The application as amended meets the requirements of the EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent in the following version:

claims: 1 to 5, filed with the letter dated 25 May 2001; 6 to 13 as attached to the communication under Rule 51(4) EPC, dated 25 January 2001,

description: pages 1 to 22 as attached to the communication under Rule 51(4) EPC, dated 25 January 2001, and page 23, filed with the letter dated 25 May 2001,

drawings: Figures 1 to 6 as attached to the communication under Rule 51(4) EPC, dated 25 January 2001.

The Registrar: The Chairman:

D. Sauter W. J. L. Wheeler