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D E C I S I O N
of 21 May 2003

Case Number: T 1216/01 - 3.4.3

Application Number: 96110018.7

Publication Number: 0736905

IPC: H01L 27/115

Language of the proceedings: EN

Title of invention:
Semiconductor device having capacitor and manufacturing method thereof

Patentee:
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 52(1), 56

Keyword:
"Inventive step (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 1216/01 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 21 May 2003

Appellant: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 6 June 2001 refusing European application No. 96110018.7 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: E. Wolff
J. H. Van Moer

Summary of Facts and Submissions

I. This is an appeal from a decision, dated 6 June 2001, in which the examining division refused European patent application Nr. 96110018.7 on the ground that claim 1 lacked an inventive step over following two documents:

D1: EP-A-503078

D2: JP-A-1-128449

II. The notice of appeal was filed on 1 August 2001. The appeal fee was paid on the same day. The statement setting out the grounds of appeal was filed on 21 September 2001.

III. In response to a communication accompanying the summons to oral proceedings of 19 March 2003, the appellant filed a new main request and two auxiliary requests, together with a further request that all dependent claims be treated as auxiliary requests.

IV. Oral proceedings took place on 21 May 2003. At the oral proceedings the appellant filed a new request which replaced all previous requests. The appellant's main request is that the decision of the examining division be rescinded and that a patent be granted on the basis of the following documents:

Claims:

– claims 1 to 3 as filed on 21 May 2003

Description:

– pages 1 to 3 and 6 to 12 as originally filed

– page 4 as filed on 18 October 1999

– page 5 as filed on 17 April 2003

Drawings:

– Sheets 1/5 to 5/5 as originally filed

Independent device claim 1 of the main request, identical in wording to claim 1 as originally filed and as rejected by the examining division, reads as follows:

"1. A semiconductor device comprising an integrated circuit (36) and a capacitor (41) formed on the integrated circuit,

wherein the capacitor comprises a bottom electrode (38) composed of a conductive layer formed on an insulating layer (37) of the integrated circuit, a capacitor dielectric layer (39) composed of one of a ferroelectric layer and a high permittivity dielectric layer formed on the bottom electrode, and a top electrode (40) composed of a conductive layer formed on the capacitor dielectric layer, and

the top electrode and bottom electrode of the capacitor are connected with interconnections (44b, 44c) of the integrated circuit through contact holes (43b, 43c) provided in an interlayer insulating layer (42) formed so as to cover the capacitor,

characterized in that the interlayer insulating layer comprises a silicon oxide layer containing phosphorous by 6% by weight or less, and the moisture content of the interlayer insulating layer is 0.5g or less per $1cm^3$."

There are no dependent device claims.

Independent method claim 2 of the main request reads as follows:

"A manufacturing method of semiconductor device comprising the steps of:

(a) forming a capacitor (41) comprising a bottom electrode (38) composed of a conductive layer, a capacitor dielectric layer (39) composed of one of a ferroelectric layer and a high permittivity dielectric layer formed on the bottom electrode, and a top electrode (10) composed of a conductive layer formed on the capacitor dielectric layer, on an insulating layer (37) of a semiconductor substrate (31) in which an integrated circuit is fabricated,

(b) forming an interlayer insulating layer (42) covering the capacitor,

(c) forming contact holes (43a, 43b, 43c) reaching the integrated circuit, and top electrode and bottom electrode of the capacitor, through the insulating layer and interlayer insulating layer,

(d) forming interconnections (44a, 44b, 44c) to be electrically connected with the integrated circuit and capacitor through the contact holes, and

(e) forming a passivation layer (45) covering the interconnections,

characterized in that the interlayer insulating layer comprises a silicon oxide layer containing phosphorus by 6% by weight or less, and

further characterized by a step carried out between steps (b) and (d) of heat treating the interlayer insulating layer prior to forming the interconnections (44a, 44b, 44c), said heat treatment being carried out in one of (i) nitrogen gas, (ii) inert gas and (iii) vacuum, so as to reduce the moisture content of said interlayer insulating layer (42) to 0.5g or less per cm^3."

Claim 3 is the only claim dependent upon claim 2.

V. The arguments presented by the appellant can be summarised as follows.

Independent device claim 1 and independent method claim 2 require that the moisture content of the interlayer insulating layer (42) formed to cover at least the capacitor of the device, is at or below

0.5g/cm^3, compared to the moisture content after formation of the layer of about 0.93g/cm^3.

The inventors of the claimed invention were the first to appreciate that the cause of inferior capacitor performance is "internal" moisture in the interlayer insulating layer, rather than "external" moisture penetrating into the device, because the internal moisture is released and diffuses into the dielectric of the capacitor during device fabrication steps taking place at elevated temperatures. The inventors were also the first to propose that the moisture content of the interlayer insulating layer should be reduced by heat treatment to less than 0.5g/cm^3 before forming any subsequent layers such as the passivation layer covering the device.

Although document D1 describes a device with the same structure as the claimed device, document D1 mentions neither moisture content of any of the device layers nor the problem of its release during processing at elevated temperatures, nor the adverse effects of such moisture on device performance.

Document D2 merely teaches that the phosphorous content of a PSG layer (6) should be chosen to be lower than 7.5% by weight in order to provide sufficient protection against humidity for a polysilicon layer 4. However, there is no mention of the moisture content of the layers described there.

Accordingly, a combination of document D2 and document D1 would not make the claimed invention obvious.

Reasons for the Decision

1. The appeal is admissible.

2. *Clarity, support in the description and amendments*

2.1 Clarity and support for the claims in the description were not in dispute, and the Board is satisfied that the claims are clear, concise and supported by the description as required by Article 84 EPC.

2.2 Claim 1 was amended neither during examination nor during the appeal proceedings. The amendments made to claim 2 during examination are based on the description as originally filed and were not in dispute. The amendments made to pages 4 and 5 of the description serve, respectively, to acknowledge the prior art and to provide consistency between the "summary of invention" statement and the claims. The Board is therefore satisfied that the application complies with the requirements of Article 123(2) EPC.

3. *Novelty*

3.1 Document D1 describes a semiconductor device in which a capacitor is formed having a bottom electrode (28), a ferroelectric dielectric (29) and a top electrode (32), with the capacitor being covered by an insulating interlayer film (33) except for the location of connection holes (Figure 2 and the corresponding text in column 5, line 35 to column 6, line 40). The device disclosed in document D1 thus has all the features of the invention, except for the features in claim 1 of

the application in suit, which specify that the interlayer insulating layer has a phosphorous content of 6% or less by weight and a moisture content of $0.5g/cm^3$ or less.

3.2 Document D2 discloses that a PSG film (6) with a phosphorous concentration of less than about 7.5% by weight is moisture resistant, but does not concern itself with capacitor structures. The Board, moreover, accepts the appellant's argument that this reference to humidity resistance appears to relate merely to the effect of the layer as a barrier to moisture penetration from outside, but says nothing about the moisture content of the layer itself.

3.3 The novelty of the independent claims 1 and 2 was not in dispute and in the light of the above-mentioned differences over the cited prior art, which were already acknowledged by the examining division, the Board is satisfied that the subject matter of these claims is novel over each of the cited prior art documents D1 and D2.

4. *Inventive step*

Claim 1

4.1 The nearest prior art document in respect of claim 1 is document D1. The invention claimed in claim 1 differs from the device disclosed in document D1 by the features set out in the characterising clause of claim 1, that is, in that the interlayer insulating layer comprises a silicon oxide layer containing phosphorous by 6% by weight or less, and the moisture

content of the interlayer insulating layer is 0.5g or less per cm^3.

4.2 The problem which the invention addresses is to improve the leakage current characteristics of capacitors. The solution provided by the invention as claimed in claim 1 is to use an interlayer insulating layer in which the moisture content does not exceed $0.5g/cm^3$. Figure 6 of the application in suit and the associated text of the description show a comparison between a conventional device in which the PSG insulating layer has a moisture content of $0.93g/cm^3$ (curve (a)) and a device according to the invention (curve (b)) in which the PSG insulating layer has a moisture content of $0.45g/cm^3$. As shown in Figure 6, the low moisture content of the interlayer insulating layer in a capacitor causes a significant improvement in the reliability of that capacitor.

4.3 According to the arguments presented by the appellant, which are supported by the introductory part of the description (page 4, lines 3 to 9 of the application as filed), the inventors were the first to realise that an important cause of leakage currents in capacitors is to be found in the moisture content of around $0.93g/cm^3$ in a conventionally formed interlayer insulation. During further processing steps this moisture diffuses into the ferroelectric dielectric layer of the capacitor thereby lowering its electric resistance which, in turn, leads to a rise in leakage current or a decline in dielectric strength and could thereby induce dielectric breakdown of the capacitor.

4.3.1 Document D1 is concerned with preventing deterioration of the electrical properties of capacitors in which the dielectric is a ferroelectric material. The deterioration is caused when the materials making up the upper electrode of the capacitor react with the aluminium of the wiring layer at temperatures around 300°C, in particular during annealing of the device and the formation of the final passivation layer (column 2, lines 14 to 28). The remedy provided in document D1 is to form a conducting, reaction-preventing film between the upper electrode and the wiring layer (column 3. lines 39 to 49). The reaction-preventing film is also effective against an increase of the junction leakage current as it prevents a reaction between Al and Si in the source and drain regions (column 8, lines 39 to 49). Thus, the skilled person would learn from document D1 that leakage currents resulting from a reaction between Al and Si can be prevented by providing a conductive reaction-preventing layer. Document D1 would not, however, have assisted the skilled person in identifying the moisture content of the interlayer as a cause of leakage currents.

4.3.2 Although document D1 also states that a final passivation layer can improve the long-term reliability of such devices by providing resistance to humidity (column 8, lines 5 to 11), it is clear from the context that this refers to protecting the device from humidity originating outside rather than from within the device. There is no mention in document D1 of the moisture content of the insulating interlayer nor of any effects which might be attributable to it.

4.4 Document D2 discloses that a PSG film with a phosphorous content of less than about 7.5% by weight provides good humidity resistance. As in the case of document D1, it is clear from the context that the low phosphorous content provides protection against moisture ingress from outside the device. There is no mention of the moisture content of the interlayer insulation film itself, nor of any possible effects of that moisture content.

4.5 There is no indication in the cited prior art of the problem caused by the natural moisture content of about $0.93g/cm^{3,}$ of the interlayer insulating layer, nor of the improvements in the electrical characteristics and reliability which, as shown by Figure 6, a reduction of the moisture content to $0.5g/cm^3$ or less can achieve. The Board therefore concludes that claim 1 is not obvious in the light of the cited prior art.

Claim 2

4.6 Claim 2 is an independent method claim with processing steps corresponding to each of the device features of claim 1, including the formation of the interlayer insulating layer having a moisture content of $0.5g/cm^3$ or less. In addition, the claim specifies that the moisture content of the interlayer insulating layer is to be reduced by heat treating the interlayer before either the interconnections or the passivating layer (45) are formed.

4.7 Document D2 discloses a method of forming a flat PSG interlayer insulating layer which also has humidity resistance. However, as already discussed in relation

to claim 1 above, the humidity resistance concerned is unrelated to the moisture content of the layer. Annealing is not referred to in document D2.

4.8 Document D1 refers to annealing, i.e., heat treatment during the device manufacture, but only at the following two stages of device fabrication: either immediately after the formation of the capacitor and before the interlayer insulating layer (33) is formed (page 5, column 7, lines 8 to 18), or after the reaction-preventing TiN film 35 has been formed.

4.9 The Board accepts the appellant's argument that in the process of document D1 in the first instance annealing takes place obviously too early, i.e., prior to the formation of the interlayer, and in the second instance too late to bring about the required reduction in the moisture content to $0.5 g/cm^3$, since in the latter case annealing occurs only after at least those areas of the interlayer film which cover the capacitor are covered by the metal film, thereby trapping the moisture in the interlayer and preventing the moisture being driven off during annealing.

4.10 The Board is therefore of the view that the invention claimed in claim 2 involves an inventive step because the solution of heat treating the interlayer insulating layer to lower its moisture content to $0.5 g/cm^3$ or less before any further layers are formed, is not obvious having regard to the cited prior art which neither concerns itself with the moisture content of interlayer insulating layer nor provides any incentive for any heat treatment at that particular stage of the fabrication process.

5. In the Board's judgement, for the reasons set out above, the invention as claimed in independent claims 1 and 2 involves an inventive step as required by Articles 52(1) and 56 EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is submitted to the first instance with the order to grant a patent with the following documents:

   - **claims** 1 to 3 filed at the oral proceedings

   - **description:**
     pages 1 to 3 and 6 to 12 as originally filed,
     page 4 filed with letter of 18 October 1999,
     page 5 filed with letter of 17 April 2003

   - **drawings** as originally filed

The Registrar: The Chairman:

U. Bultmann R. K. Shukla