BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS | BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE | CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [ ] To Chairmen
(D) [X] No distribution

D E C I S I O N
of 28 May 2004

Case Number: T 1187/01 - 3.4.3

Application Number: 92101021.1

Publication Number: 0499063

IPC: H01L 23/528

Language of the proceedings: EN

Title of invention:
Resin sealed semiconductor integrated circuit comprising a wiring layer

Applicant:
NEC CORPORATION, et al

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 84, 123(2)

Keyword:
"Main request (clarity: yes)"

Decisions cited:
-

Catchword:
-

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 1187/01 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 28 May 2004

Appellant: NEC CORPORATION
7-1, Shiba 5-chome,
Minato-ku
Tokyo (JP)

Representative: Glawe, Delfs, Moll & Partner
Patentanwälte
Postfach 26 01 62
D-80058 München (DE)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 4 May 2001 refusing European application No. 92101021.1 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: V. L. P. Frank
J. P. B. Seitz

Summary of Facts and Submissions

I. The appeal lies against the decision of the Examining Division dated 4 May 2001 to refuse the European patent application No. 92 101 021.1 on the ground that claim 1 of the main, second and third auxiliary requests did not meet the requirements of Article 123(2) and 84 EPC and that claim 1 of the first auxiliary request did not meet the requirements of Article 84 EPC.

II. The appellant (applicant) lodged an appeal against the above decision on 4 July 2001, paying the appeal fee the same day. The statement setting out the grounds of appeal was filed on 14 September 2001. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the claims according to a main and first to fourth auxiliary requests submitted with the statement of grounds of appeal.

III. During the oral proceedings before the Board which took place on 28 May 2004, the appellant replaced his previous requests by a new main request and an auxiliary request, as follows:

(i) **Main Request:**

Claims: 1 to 4, as filed during the oral proceedings on 28 May 2004

Description: pages 3 and 8 to 10, as originally filed
pages 1, 2, 4, 5, 5a, 6 and 12, as filed with letter of 26 May 2000,
pages 7, 11 and 13, as filed during the oral proceedings on 28 May 2004

Drawings: Figures 1A, 1B, 2 and 3, as originally filed.

(ii) Auxiliary request:

Claims: 1 to 3, as filed during the oral proceedings on 28 May 2004

The wording of the independent claims of these requests is as follows:

Main request:

"1. A resin sealed semiconductor integrated circuit having a square or rectangular semiconductor chip comprising a semiconductor substrate (101) having a corner, a bonding pad (209A) formed on an insulating film (107) covering said semiconductor substrate near said corner of said semiconductor substrate, a wiring layer (208) extended from said bonding pad and elongated on said insulating film in a predetermined direction, said wiring layer having a first portion (I) near to said bonding pad and a second portion (II) far from said bonding pad, a first plurality of slits (S) formed in said first portion of said wiring layer and extending in the predetermined direction to form a plurality of first wiring segments, a passivation film (110) covering said wiring layer and said insulating film, said first wiring segments being extended in parallel to each other in said predetermined direction and each having a first width,
characterized by a second plurality of second slits (s) formed in said second portion of said wiring layer and extending in the predetermined direction to form a

plurality of second wiring segments, said second wiring segments being extended in parallel to each other in said predetermined direction and each having a second width, said first width being smaller than said second width, wherein the total width of said first portion is greater than the total width of said second portion."

The independent claim 1 according to the auxiliary request adds at the end of claim 1 of the main request the feature:

"wherein each of said first and second slits has a width greater than twice a width of a thickness of said passivation layer."

IV. The arguments of the Examining Division insofar as they are relevant to the present requests can be summarized as follows:

(a) The object of the invention is to prevent sliding and/or destruction of the wiring. As disclosed in the application on page 10 line 17 to page 11, line 2, the maximum allowable width (Wmax) of the wiring segments depends on the distance (X) to the closest corner of the chip and has to satisfy the inequality $W \leq 17.6 + X/82$ to avoid sliding or destruction of the wiring. Moreover, as disclosed in the application the width of the slits has to be at least twice the thickness of the passivation layer in order to be filled without voids, which lead to the formation of cracks in the passivation layer.

As the independent claim does not contain these features, it does not meet the requirements of Article 84 EPC taken in combination with Rules 29(1) and (3) EPC that any independent claim must contain all the technical features essential to the invention.

(b) The application documents as filed do not comprise a clear definition of the total width of the wiring or wiring portion. It is not clear from the application whether the total width is the sum of the wiring segments width, or if it is sum of the wiring segments width and the slit widths. Therefore, the specification in the claim that the total widths of the first portion is greater than the total width of the second portion renders the claim unclear (Article 84 EPC).

V. The arguments of the appellant can be summarized as follows:

(a) The condition specified in the description on pages 10 to 11 on the maximum allowable width of the wiring layer to prevent sliding is estimated on the basis of tests on a specific semiconductor chip sealed to a Small Outline Package. There is no suggestion in the application that this limitation is an essential feature of the invention nor that it is valid for other semiconductor chips and/or packages.

(b) Similarly the requirement that the slits have a given width, i.e. twice the thickness of the passivation layer, is merely a particular

preferred embodiment of the invention. There are methods well known to the skilled person to fill slits which are narrower than twice the thickness of the overlying passivation film.

Reasons for the Decision

1. The appeal is admissible.

2. The application in suit addresses the problem of wiring sliding and/or destruction in a resin sealed semiconductor integrated circuit. The wiring layer is usually an aluminium or aluminium alloy film which is formed on top of an insulating film and covered by a passivation film. The passivation film prevents ingress of moisture and contaminants from the sealing resin. It is, therefore, essential to prevent cracking of the passivation film not only during manufacturing of the chip but also through its lifetime. However, due to the different thermal expansion coefficients of the resin and the semiconductor chip, stresses are generated upon cooling of the resin and also during thermal cycling of the chip. This stress, which is directed to the centre of the chip, increases with distance from the centre and is largest at the chip's periphery. The power or ground wiring layers are, however, located on the chip's periphery, are subjected to this increased stress and are liable to slide, producing cracks in the overlying passivation film (cf. pages 1 and 2 of the application in suit).

In order to overcome the above mentioned problem of wire sliding and/or destruction the application in suit

proposes to provide slits in the wiring layer, thereby reducing the effective width of the wiring and providing anchoring points between the passivation and insulating layers within the area of the wiring layer.

A relatively large wiring's cross section, however, is required to reduce electromigration in the aluminium layer, since electromigration is directly proportional to the current density traversing the wiring. As wiring side branches (208Aa, 208Ab, 208Ac) divert current to the different active regions on the chip, the wiring's cross section, i.e. the total width of the wiring layer, may be reduced non-continuously with increasing distance to the bonding pad in order to reduce the space occupied by the wiring layer on the chip's periphery. (cf. page 6, line 20 to page 7, line 2; Figure 3).

3. *Main request*

3.1 Clarity

3.1.1 The Board concurs with the appellant that the upper limit for the width (W) of the wiring layer in relation to its distance (X) from the chip's corner as disclosed in the paragraph bridging pages 10 and 11, i.e. $W \leq 17.6 + X/82$, so as to avoid wire sliding is applicable only in case of a particular chip's size and packaging and, that there is no suggestion in the application in suit that it is an essential condition for chips of different dimensions or for a different type of packaging.

Also the feature that the width of the slits should be twice the thickness of the passivation layer cannot be regarded as essential for the performance of the invention, since, according to the appellant, there are several deposition methods available to the skilled person for filling narrow slits. This feature is, moreover, specified in the description as merely a preferred embodiment of the invention (cf. page 6, lines 17 to 19).

In the Board's view, therefore, claim 1 contains all the essential features of the invention as described.

3.1.2 The Board is also not able to follow the Examining Division's argumentation that the expression "total width of the wiring layer" is not clear (Article 84 EPC). The argument that according to the application in suit it is uncertain whether the total width of the wiring layer means the sum of the widths of the wiring segments or the sum of the widths of the wiring segments and of the slits is not substantiated in the contested decision nor in the previous communications by citing the application's passages from which this uncertainty arises.

In interpreting a claim the words have to be assigned their normal meaning unless there are special reasons for departing from this, eg particular definitions assigning a special meaning to some expressions. In the present context, the expression the "total width" of the wiring layer can only mean the width as measured from one side of the wiring layer to the other, i.e. the sum of the wiring segment's and slits widths. No

other interpretation of this expression seems sensible under the present circumstances.

3.1.3 For these reasons, the Board concludes that claim 1 according to the main request complies with Article 84 EPC.

3.2 Article 123(2) EPC

The wiring layer according to claim 1 of the main request comprises a first (I) and a second (II) portion which are, respectively, near and far from the bonding pad. In both portions slits (S) are formed which divide the wiring layer into several wiring segments (208A-1 and 208A-2) (cf. Figure 3). The width of the wiring segments in the first portion is smaller than that of the second portion, to counteract the larger sliding force which is exerted close to the chip's corner where the bonding pad is located. It is further specified in the claim that the total width of the wiring layer's first portion is larger than that of the second portion, thus saving space of the chip.

The above features of the wiring segments are derived from the embodiment of the invention as described with reference to Figure 3 (cf. page 11, line 23 to page 12, line 19). The feature that the total width of the wiring layer decreases non-continuously with increasing distance to the bonding pad is disclosed *inter alia* on page 6, lines 8 to 13.

Since the invention as defined in amended claim 1 contains features which are disclosed in the application in suit, and since it is also consistent

with the invention as described as regards the essential features required to solve the problem of wire sliding, claim 1 as amended complies with Article 123(2) EPC.

4. In the proceedings before the Examining Division no objections were raised with respect to the novelty or inventive step of the subject-matter as claimed. None of the state of the art documents cited in the European Search Report addresses the problem of sliding and/or destruction of the wiring layer in the proximity of the chip's corners nor the problem of reducing the space occupied by the wiring layer.

In particular, EP-A-0 223 698 discloses to divide a busbar into several parallel strips of smaller width (about 3 µm) to reduce the occurrence of hillocks in a metallization layer, as the hillocks may cause a short circuit between one wiring layer and an overlying wiring layer.

US-A-4 467 345, on the other hand, discloses to reduce the width of the wiring layer in order to limit the grain size of the phosphosilicate glass which can grow on the aluminium metallization layer, since large grain size may produce cracks in the passivation layer.

These documents, however, do not disclose wiring segments which have a variable width depending on the distance to the bonding pad.

The Board is, for these reasons, satisfied that the subject-matter of the claims according to the main

request are new and involve an inventive step (Article 52(1), 54 and 56 EPC).

5. Therefore, in the judgment of the Board the appellant's main request fulfils the requirements of the EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent with the following documents:

Claims: No. 1 to 4 of the main request filed during the oral proceedings of 28 May 2004.

Description: pages 3, 8 to 10, as originally filed
pages 1, 2, 4, 5, 5a, 6 and 12, as filed with the letter of 26 May 2000,
pages 7, 11 and 13, as filed during the oral proceedings of 28 May 2004.

Figures: 1A, 1B, 2 and 3, as originally filed.

The Registrar: The Chairman:

D. Meyfarth R. K. Shukla

1489.D