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D E C I S I O N
of 25 November 2003

Case Number: T 1117/01 - 3.5.2

Application Number: 98950557.3

Publication Number: 1025640

IPC: H03H 7/30

Language of the proceedings: EN

Title of invention:
Integrated electronic circuit comprising an oscillator and passive circuit elements

Applicant:
Bofors Defence AB

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56, 84

Keyword:
"Claims - clarity (after amendment - yes)"
"Inventive step - (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 1117/01 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 25 November 2003

Appellant: Bofors Defence AB
S-691 80 Karlskoga (SE)

Representative: Splanemann Reitzner Baronetzky Westendorp
Patentanwälte
Rumfordstrasse 7
D-80469 München (DE)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 30 April 2001 refusing European application No. 98950557.3 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: M. Ruggiu
J. H. P. Willems

Summary of Facts and Submissions

I. The applicant filed an appeal against the decision of the examining division to refuse European patent application No. 98 950 557.3, which had been filed as an application under the PCT published under No. WO 99/21274.

II. Reasons given for the refusal were that the subject-matter of claim 1 was unclear, contrary to Article 84 EPC, and that the subject-matter of claims 1 to 13 did not involve an inventive step in the sense of Article 56 EPC.

III. The decision under appeal cited the following prior art documents:

D1: US-A-5 652 549;

D2: WO-A-94/17558;

D3: US-A-5 561 434; and

D4: US-A-4 757 318.

IV. Oral proceedings were held before the board on 25 November 2003, at which the appellant amended the claims and the description. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the following documents:

Description: pages 1, 2, 2a, 5 and 6 filed during the oral proceedings;
pages 3, 4 and 7 to 10 of WO 99/21274;

Claims: No. 1 to 17 filed during the oral proceedings;

Drawings: sheets 1/3 to 3/3 of WO 99/21274.

V. Claim 1 reads as follows:

"An integrated electronic circuit comprising a delay element formed by an electric conductor (13, 18) and at least one active electronic component (10, 21) connected to said electric conductor (13, 18), wherein said conductor (13, 18) is formed such that its inductance is minimized, i.e. in a loop with parallel conductor sections so that the directions of the current in adjacent conductor sections are opposite to each other and said conductor (13, 18) is formed by a conductive material on an insulating layer (14), characterized in that the insulating layer (14) is surrounded by semiconducting material (15) and the thickness of the insulating layer (14) exceeds 10 µm so as to provide a low capacitive coupling between the conductor (13, 18) and the surrounding semiconducting material."

Claims 2 to 17 are dependent on claim 1.

VI. The appellant essentially argued as follows:

The amendments made to claim 1 clarified the terms "minimized" and "surroundings". The term "low

capacitive coupling" was clear in the context of claim 1, because this term had no other technical significance than to indicate the aim achieved by having a thickness of the insulating layer in excess of 10 µm.

The prior art closest to the invention was disclosed in document D1 which concerned an integrated electronic circuit in bipolar technology. A delay element of the circuit of D1 comprised a double line on an insulating layer, which double line was formed by aluminium tracks with a mutual spacing of 2 µm. This structure provided a comparatively high but well defined capacitance, which resulted in a relatively high attenuation of the signal in the delay element. This made the circuit of D1 less suitable for use in applications where the signal levels were low, such as in antenna receiving circuits. Contrary to the approach followed in D1, the invention decreased the effects of the variation of the capacitance by providing a delay element with a low capacitance, which performed well in low-level applications such as in antennas. The normal thickness for the insulation between metallization levels in a circuit made with the technology indicated in D1 would be about 1 µm. Using a thicker insulation would involve a substantial modification of the existing technology and thus would not be obvious to the skilled person. Furthermore, the mention in D1 of a 2 µm spacing between the tracks indicated to the skilled person that a 2 µm thick insulating layer would be sufficient to insulate the double line from the semiconducting material of the integrated circuit.

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments*

2.1 According to page 5, lines 7 to 10, of the application as originally filed (WO 99/21274), the conductor preferably runs in a loop with several parallel conductor sections as specified in present claim 1. Furthermore, passages of WO 99/21274 at page 4, lines 25 to 28, and page 9, lines 22 to 26, indicate that the conductor rests on some form of insulating layer and that semiconducting material, for example silicon, surrounds the portion that supports the conductor. The other features recited in present claim 1 are contained in claim 1 as originally filed. Thus, the subject-matter of present claim 1 does not extend beyond the content of the application as filed.

2.2 The dependent claims and the description have been amended for consistency with present claim 1. The description has also been amended to acknowledge the prior art disclosed in document D1.

2.3 Therefore, the amendments to the application do not contravene Article 123(2) EPC:

3. *Clarity*

According to present claim 1, the thickness of the insulating layer exceeds 10 µm so as to provide a low capacitive coupling between the conductor and the surrounding semiconducting material. The term "low

capacitive coupling" merely specifies the aim to be achieved by having a thickness of the insulating layer exceeding 10 µm and does not require that the capacitance between the conductor and the surrounding semiconducting material be lower than some specific value. Thus, the board regards this term as clear in the context of present claim 1 and considers that claim 1 meets the requirement of Article 84 EPC.

4. *Novelty*

4.1 Document D1 discloses an integrated electronic circuit in B6HF bipolar technology having the features recited in the preamble of claim 1. The delay element of the circuit of D1 comprises aluminium tracks proceeding in a third metallization layer of the circuit over a metal surface, formed in a first metallization layer, lying at ground potential. The metallization layers are insulated by silicon dioxide. D1 does not specify the thickness of the insulating layer that supports the tracks (which correspond to the conductor of present claim 1). However, in view of the technology specified in D1, it can be assumed that this thickness is significantly lower than 10 µm. Furthermore, since the tracks are part of a metallization layer, the corresponding insulating layer would apparently not be surrounded by semiconducting material, which means that the structure of the delay element of D1 is different from that recited in present claim 1.

4.2 Document D2 concerns integrated circuits having monolithic passive components. D2 describes in particular an inductor 12 taking the form of a loop with parallel conductor sections, wherein the current

in adjacent sections has the same direction and not opposite directions as specified in present claim 1. The inductor 12 is suspended over a pit 14 formed in a 500 µm thick silicon substrate 16. The inductor 12 is encapsulated and supported by a bridge structure formed from a 2 µm thick insulating silicon dioxide layer 20 overlying the substrate 16 (see especially Figure 2 of D2). D2 also indicates at page 15, lines 25 to 29, that capacitors can be formed in the insulating layer and positioned over a pit in the substrate to reduce losses induced by the substrate. To form a capacitor, spaced parallel sheets are deposited in the oxide layer. Thus, D2 does not disclose a delay element as specified in present claim 1.

4.3 Documents D3 and D4 concern phased array antennas with delay elements. D3 indicates that the delay elements take the form of microstrips while D4 remains silent on the technology used to implement the delay elements. Thus, neither of D3 and D4 discloses an integrated circuit comprising a delay element.

4.4 Thus, the subject-matter of claim 1 does not form part of the cited state of the art. It is therefore considered to be new (Article 54(1) EPC).

5. *Inventive step*

5.1 The board concurs with the appellant and the examining division in regarding D1 as the closest prior art from which to start the assessment of inventive step. The subject-matter of claim 1 differs from this closest prior art in that the insulating layer is surrounded by semiconducting material and the thickness of the

insulating layer exceeds 10 µm so as to provide a low capacitive coupling between the conductor and the surrounding semiconducting material. This apparently makes the integrated delay element of the invention suitable for applications with weak signals such as in receiving antennas.

5.2 The integrated delay element of D1 is formed by two metallization layers separated by silicon dioxide. Thus, D1 does not suggest the structure recited in present claim 1, comprising conductive material on an insulating layer surrounded by semiconducting material. In view of the technology used for the integrated circuit of D1, the skilled person would regard a thickness of the order of 1 or 2 µm as sufficient for the insulation disposed between metallization layers and would have no reason to depart from it. This is supported by the indication in D1 that the spacing between the conducting tracks, which must be insulated from one another, can be a mere 2 µm. The skilled person would consider such a spacing as adequate for the insulation of the tracks and thus for the thickness of the insulating layer.

5.3 Document D2 does not disclose a delay element. The capacitor described in D2 is formed by spaced, parallel sheets of metallization that are deposited in an oxide layer, which, as shown in Figure 2 of D2, has a thickness of 2 µm. D2 therefore does not go beyond what is disclosed in D1.

5.4 Documents D3 and D4 do not describe integrated electronic circuits. Therefore, D3 and D4 would not be considered by the skilled person looking to solve a problem relating to an integrated delay element.

5.5 Thus, the skilled person would not be led by the cited documents to modify the structure of the delay element disclosed in D1 and to increase the thickness of the insulation provided there. Having regard to the state of the art, the subject-matter of present claim 1 is therefore not obvious to a person skilled in the art and is to be considered as involving an inventive step in the sense of Article 56 EPC.

6. Claims 2 to 17 are dependent on claim 1. Thus, the subject-matter of claims 1 to 17 is also considered as being new and involving an inventive step.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent in the following version:

Description: pages 1, 2, 2a, 5 and 6 filed during the oral proceedings;
pages 3, 4 and 7 to 10 of WO 99/21274;

Claims: No. 1 to 17 filed during the oral proceedings;

Drawings: sheets 1/3 to 3/3 of WO 99/21274.

The Registrar:

D. Sauter

The Chairman:

W. J. L. Wheeler