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D E C I S I O N
of 17 February 2004

Case Number: T 0910/01 - 3.5.2

Application Number: 96908502.6

Publication Number: 0759230

IPC: H03G 3/00

Language of the proceedings: EN

Title of invention:
CMOS PROGRAMMABLE RESISTOR-BASED TRANSCONDUCTOR

Applicant:
LATTICE SEMICONDUCTOR CORPORATION

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56, 84

Keyword:
"Clarity of claims - yes (after amendment)"
"Inventive step - yes"

Decisions cited:
-

Catchword:
-

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Case Number: T 0910/01 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 17 February 2004

Appellant: LATTICE SEMICONDUCTOR CORPORATION
5555 N.E. Moore Court
Hillsboro,
Oregon 97124 (US)

Representative: Atkinson, Ralph
Atkinson Burrington
25-29 President Buildings
President Way
Sheffield S4 7UR (US)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 6 February 2001 refusing European application No. 96908502.6 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: R. G. O'Connell
C. Holtz

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division to refuse application No. 96 908 502.6. The reasons given for the refusal were that dependent claims 6 and 8 effectively claimed the same subject-matter so that the claims were not clear and concise and that the subject-matter of claim 1 did not involve an inventive step, having regard to the prior art known from

D1: US-A-4 667 166 and

D2: E.D.N. Electrical Design News, vol. 32, No. 2, 22 January 1987, pages 181 to 187, A. Kaniel: "Flexible PGA designs require few components".

II. Following a communication accompanying summons to oral proceedings, the appellant filed amended claims 1 to 10 and amended pages 1 to 6 of the description. The oral proceedings were cancelled.

III. The appellant requests that the decision under appeal be set aside and that a patent be granted in the following version:

- Claims 1 to 10 filed with the letter of 26 January 2004;

- Description: pages 1 to 4 and 6 filed with the letter of 26 January 2004, page 5 filed with the letter of 3 February 2004, and pages 7 to 14 of the published application (WO 96/27239); and

– Drawings: sheets 1/4 to 4/4 of the published application.

IV. Claim 1 is now worded as follows:

"A programmable transconductor for generating a differential current between a first current output terminal and a second current output terminal, wherein said differential current is responsive to a differential voltage operably impressed between a first voltage input terminal and a second voltage input terminal, wherein

a current source circuit (30) configured to deliver a predetermined amount of current into each of a first summing node and a second summing node;

a first gain block (44) has a first input coupled to said first voltage input terminal, a second input coupled to a first feedback node (60) and an output;

a first transistor (46) has a first current-handling terminal coupled to the first summing node, a second current-handling terminal coupled to said first current output terminal and a control terminal coupled to the output of said first gain block;

a second gain block (54) has a first input coupled to said second voltage input terminal, a second input coupled to a second feedback node (70) and an output; and

a second transistor (56) has a first current-handling terminal coupled to a second summing node, a second current-handling terminal coupled to said second current output terminal and a control terminal coupled to the output of said second gain block,

a resistor circuit (RMID, R1, R2) is coupled between said first summing node and said second summing node, said resistor circuit comprising a plurality of individual resistors connected in series and defining a plurality of intermediate nodes between adjacent resistors; characterised by

a first plurality of switch circuits (S1, S2, S3), each having a first terminal coupled to a corresponding node of the resistor circuit (36, 67, 68) and each further having a second terminal coupled to the first feedback node (60); and

a second plurality of switch circuits (S1, S2, S3), each having a first terminal coupled to a corresponding node (38, 77, 78) of the resistor circuit, and each further having a second terminal coupled to the second feedback node (70); wherein

the resistor circuit and the plurality of switch circuits are configured to provide a programmable transconductance gain."

Claims 2 to 10 are dependent on Claim 1.

V. The appellant's arguments may be summarized as follows. In order to overcome the objection of lack of clarity and conciseness, claim 6 has been amended and former

claim 8 has been deleted, former claims 9 to 11 being consequentially renumbered as claims 8 to 10. The present invention related to a programmable transconductor which received first and second input voltages and generated first and second output currents whose magnitudes were proportional to respective ones of the input voltages. The difference between the output currents was proportional to the difference between the input voltages. Using a resistor to set the transconductance gain of a transconductor resulted in a high linearity, but the gain was fixed by the resistor value and varied with semiconductor process parameter variations. In the present invention, the transconductance gain was changeably selectable after semiconductor manufacturing.

D1 disclosed a differential amplifier system with voltage divider means in the feedback path of the gain blocks for reducing the range of voltages handled by the differential amplifiers and lessening the adverse effects of the stray capacitances of their inputs. There was no disclosure in D1 that the voltage divider means could be used to provide a programmable transconductance gain. In D2, figure 2 showed differential programmable gain amplifiers with programmable resistances in the feedback loops of operational amplifiers. If this teaching were applied to the differential amplifier system of D1, it would not influence the transconductance gain and would not result in a circuit arrangement according to the present claim 1.

Reasons for the Decision

1. The appeal is admissible.

2. The features recited in the present claims are all disclosed in claims 1 to 11 of the application WO 96/27239 as filed and supported by the description, page 6, line 22 to page 14, line 4. Pages 1 to 6 of the description have been adapted to the present claims and amended to acknowledge the prior art known from D1. The amendments do not contravene Article 123(2) EPC and they overcome the examining division's objection to lack of clarity and conciseness.

3. The closest prior art among the documents cited by the examining division is D1, which discloses with reference to its figure 5 a differential amplifier system for generating a differential current between a first current output terminal (collector of transistor 42) and a second current output terminal (collector of transistor 44), wherein said differential current is responsive to a differential voltage operably impressed between a first voltage input terminal (12) and a second voltage input terminal (14), wherein:

   – a current source circuit (the two current sources I_0) is configured to deliver a predetermined amount of current into each of a first summing node (emitter of transistor 16) and a second summing node (emitter of transistor 18);

– a first gain block (66) has a first input (+) coupled to said first voltage input terminal (12), a second input (-) coupled to a first feedback node (between resistors 76 and 78) and an output;

– a first transistor (16) has a first current-handling terminal coupled to the first summing node, a second current-handling terminal coupled to said first current output terminal and a control terminal coupled to the output of said first gain block;

– a second gain block (68) has a first input (+) coupled to said second voltage input terminal (14), a second input (-) coupled to a second feedback node (between resistors 78 and 80) and an output;

– a second transistor (18) has a first current-handling terminal coupled to the second summing node, a second current-handling terminal coupled to said second current output terminal and a control terminal coupled to the output of said second gain block; and

– a resistor circuit (R1, 76, 78, 80) is coupled between said first summing node and said second summing node, said resistor circuit comprising a plurality of individual resistors connected in series and defining a plurality of intermediate nodes between adjacent resistors.

4. The subject-matter of claim 1 differs from the prior art known from D1 in that it is a programmable transconductor, having:

– a first plurality of switch circuits, each having a first terminal coupled to a corresponding node of the resistor circuit and each further having a second terminal coupled to the first feedback node; and

– a second plurality of switch circuits, each having a first terminal coupled to a corresponding node of the resistor circuit, and each further having a second terminal coupled to the second feedback node; wherein

the resistor circuit and the plurality of switch circuits are configured to provide a programmable transconductance gain.

5. The advantage brought by these characterising features is that the transconductance gain is changeably selectable after semiconductor manufacturing.

6. D2 discloses various programmable gain amplifiers (PGAs). A differential PGA is shown in figure 2a with programmable resistances (H1508) in the feedback loops of operational amplifiers. If this teaching were applied directly in a straightforward manner to the differential amplifier system of D1, the resulting circuit would have a programmable resistance connected directly between the output of each of the operational amplifiers (66, 68) and its inverting input, so that the voltage gain of each of these amplifiers would be individually programmable. The resulting circuit would not have an arrangement of first and second switch circuits according to the characterising part of

claim 1. Furthermore, even if it were assumed (to the appellant's disadvantage) that it was obvious to couple the programmable resistances between the respective feedback nodes and the inverting inputs of the operational amplifiers (66, 68), this would also not result in an arrangement of first and second switch circuits according to the characterising part of claim 1.

7. In the judgement of the Board, there is nothing in the prior art (D1 and D2) cited by the examining division which would make it obvious to the skilled person to modify the circuit shown in figure 5 of D1 by replacing the fixed resistors 76 and 80 by programmable resistances and configuring the circuit to provide a programmable transconductance gain in the manner specified in the characterising part of claim 1 of the present application.

8. The Board therefore concludes that the subject-matter of claim 1 shall be considered as involving an inventive step in accordance with Article 56 EPC.

9. The Board finds that the application meets the requirements of the EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

   – Claims 1 to 10 filed with the letter of 26 January 2004;

   – Description: pages 1 to 4 and 6 filed with the letter of 26 January 2004, page 5 filed with the letter of 3 February 2004, and pages 7 to 14 of the published application (WO 96/27239); and

   – Drawings: sheets 1/4 to 4/4 of the published application.

The Registrar: The Chairman:

D. Sauter W. J. L. Wheeler