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D E C I S I O N
of 22 February 2006

Case Number: T 0824/01 - 3.5.03

Application Number: 96102106.0

Publication Number: 0726571

IPC: G11B 20/10

Language of the proceedings: EN

Title of invention:
Decoder/encoder capable of controlling data reading/writing operations to memory in response to first/second clocks, reproducing apparatus equipped with encoder/decoder, and recording apparatus equipped with encoder

Applicant:
SONY CORPORATION

Opponent:
-

Headword:
Decoder and encoder/SONY

Relevant legal provisions:
EPC Art. 56, 84, 123(2)

Keyword:
"Inventive step (main and auxiliary requests) - no"

Decisions cited:
-

Catchword:
-

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Case Number: T 0824/01 - 3.5.03

D E C I S I O N
of the Technical Board of Appeal 3.5.03
of 22 February 2006

Appellant: SONY CORPORATION
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 28 February 2001 refusing European application No. 96102106.0 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: A. S. Clelland
Members: A. J. Madenach
R. Moufang

Summary of Facts and Submissions

I. This is an appeal against the decision by the examining division to refuse European Patent Application No 96102106.6 posted on 28 February 2001.

II. The appeal was filed on 19 April 2001, with the statement of grounds being filed on 13 June 2001. The appellant requested that the impugned decision be set aside and a patent be granted on the basis of claims as filed with the statement of grounds.

III. In communications of 26 November 2004, 15 April 2005 and 8 November 2005, the board gave its preliminary opinion on the case under appeal. The appellant filed amended requests on 8 March 2005 and on 1 August 2005.

IV. Oral proceedings were arranged for 22 February 2006. In a letter of 23 January 2006, the appellant submitted new claims 1 and 7 of both main and auxiliary requests.

V. During the oral proceedings, the appellant confirmed the request that the impugned decision be set aside and a patent granted based on claims 1 and 7 according to the main or alternatively according to the auxiliary request as filed with letter of 23 January 2006, with claims 2-6 and 8-12 as filed with letter of 1 August 2005 for both requests.

At the end of the oral proceedings, the chairman announced the board's decision.

VI. The examining division in their decision relied on documents

D1: EP 429139 A
D2: US 4536864 A

and considered D1 as the closest prior art document. According to this decision, D1 showed all features of the then claims 1 and 8 apart from the feature that the decoder/encoder circuit is part of a shock proof system. It was stated that D1 disclosed a circuit, which "may be employed in any recording and read system in which a scanning means can be moved to a previous portion of the track", the storage capacity of the buffer being selected to be adequate "to compensate for the resulting fluctuations in the amount of information stored". The skilled person looking for an alternative to the shock-proof system as described in D2 and knowing the requirements for such a system would, it was argued, consider the system of D1 for this purpose since it exactly fulfilled these requirements.

VII. The appellant argued in the statement of grounds of appeal that such an argument was based on hindsight, in particular since in D1 the subject-matter of D2 was discounted.

VIII. Independent claim 1 of the main request reads as follows:

"A decoder circuit of a shock-proof system comprising:

first signal processing means (30) for performing a predetermined signal processing to data read out from a recording medium (11) based upon a first clock;

first clock generating means (7; 32; 71) for generating said first clock,

storage means (27; 28) for temporarily storing therein the data processed by said signal processing means,

write control means (50) for writing said signal-processed data into said storage means (27; 28) based on said first clock,

second clock generating means (80) for generating a stabilized second clock (MCK) independent of and different from said first clock;

read control means (50) for reading out the data stored in said storage means (27; 28) based on said second clock (MCK);

and

second signal processing means (61) for expanding the signal-processed data read out by said read control means (50), said second signal processing means (61) being controlled on the basis of said second clock (MCK),

wherein said first clock (GCK) is generated in synchronism with the operation of the recording medium (11)."

Claim 4 of the main request defines a reproducing apparatus comprising a decoder circuit according to claim 1 or claim 2.

Independent claim 7 of the main request reads:

"An encoder circuit of a shock-proof system comprising:

storage means (27; 28) for temporarily storing therein input data;

first clock generating means (71) for generating a first clock,

read control means (50) for reading out the data stored in said storage means (27; 28) based on said first clock;

first signal processing means (30) for performing, based upon said first clock, a predetermined signal processing to the data read out from said storage means (27; 28);

second clock generating means (80) for generating a stabilized second clock (MCK) independent of and different from said first clock;

second signal processing means (62) for compressing the inputted data, said second signal processing means (62) being controlled on the basis of said second clock (MCK);

and

write control means (50) for writing said compressed input data into said storage means (27; 28) based on said second clock (MCK);

wherein said first clock (GCK) is generated in synchronism with the operation of the recording medium (11)."

Claim 10 of the main request defines a recording apparatus comprising an encoder circuit according to claim 7.

Independent claim 1 of the auxiliary request adds the following features to claim 1 of the main request:

"said read control means (50) being adapted to perform the data reading operation from said storage means (27; 28) by designating the read out address by controlling

a read pointer, wherein said read pointer is incremented continuously"

and

"said write control means being adapted to restart the operation of reading out data from said recording medium (11) and to increment the write pointer which designates the data write address of said storage means (27; 28), if the data storage amount of said storage means (27; 28) becomes lower than a predetermined data amount at a certain time instant".

Independent claim 7 of the auxiliary request adds the following features to claim 7 of the main request:

"said write control means (50) being adapted to perform the data writing operation from said storage means (27; 28) by designating the write address by controlling a write pointer, said write pointer being incremented continuously"

and

"said read control means (50) is adapted to restart the operation of recording data on said recording medium (11) and to increment the read out write (sic) pointer which designates the data read out address of said storage means (27; 28), if the data storage amount of said storage means (27; 28) becomes more than a predetermined data amount at a certain time instant".

Reasons for the Decision

1. *Amendments (Article 123(2) EPC)*

1.1 The decoder and encoder circuits respectively claimed in claims 1 and 7 of the main request are in essence disclosed in original claims 6 and 15, with the feature "of a shock-proof system" being disclosed in various parts of the original description (e.g. col. 12, lines 23-25 of the application as published).

The feature of the second clock generating means being "independent of ... said first clock" can be derived from any of the Figures 4, 5, 7-10 where the second clock (reference numerals 8, 80) is shown independently of the first clock (reference numerals 7, 32, 42) in combination with the disclosure at col. 17, l. 33-36 of the application as published, which reads the "PLL data clock ... is such a clock containing the rotation jitter component of the disk". Since rotation jitter is caused by an external influence the PLL data clock (which corresponds to the first clock) cannot be derived from a master clock in the same way as the second clock. It must, therefore, be independent of the second clock.

All further amendments to original claims 6 and 15 can be derived in a straightforward manner from the Figures and description.

1.2 The board is satisfied that the features added by claims 1 and 7 of the auxiliary request can be derived from col. 14, l. 37 to col. 15, l. 2 of the application as published.

1.3 The board, therefore, accepts that claims 1 and 7 of the main and the auxiliary requests satisfy the requirements of Article 123(2) EPC.

2. *Interpretation of claims*

2.1 The board interprets the claims to "a decoder circuit of a shock-proof system" in claim 1 of both requests and "an encoder circuit of a shock-proof system" in claim 7 of both requests as being directed to a decoder/encoder **suitable for** a shock-proof system.

Moreover, the board observes that in the context of the application in suit, the property of being "shock-proof" arises from the provision of a sufficiently large buffer memory in the decoder/encoder (col. 12, l. 23-27), i.e. it is a property of the decoder/encoder itself. The reference to a decoder/encoder "of a shock-proof system" is not therefore understood as encompassing system features beyond the decoder/encoder of the claimed subject-matter.

2.2 It is to be noted that in the art the actual size of a buffer memory for a shock-proof system is determined by a trade-off between recording/reading reliability and memory cost, and is in principal only sufficient to compensate for a shock of predetermined size. Thus, whether a memory is sufficiently large for an decoder/encoder to be classified as shock-proof is a matter of degree, and the expression is therefore of unclear limitative effect as regards the size of the buffer memory.

2.3 The board observes that the final feature of claims 1 and 7 of both requests, that the first clock is generated "in synchronism with the **operation** of the recording medium" (emphasis by the board), is interpreted in a very broad sense as it not clear from the claims what type of recording medium and what operation are meant.

The appellant in his letter of 23 January 2006 indicated an intention to restrict the "recording medium" to "disk recording medium" and the "operation" to "reading the groove information from the disk".

Although no request based on these limitations was submitted, the board has taken them into account when considering the question of inventive step (see point 3.2 below).

3. *Inventive step, main request (Article 56 EPC)*

3.1 D1, which is considered to represent the single most relevant prior art document, discloses in Figures 1 and 5b a decoder circuit comprising: first signal processing means (51 in Fig. 5b) for performing a predetermined signal processing to data read out from a recording medium (2) based upon a first clock; first clock generating means (9) for generating said first clock; storage means (11) for temporarily storing therein the data processed by said signal processing means; and second clock generating means (8) for generating a second clock; second signal processing means (12a in Fig. 5b) for expanding the signal-processed data, said second signal processing means being controlled on the basis of said second clock;

wherein said first clock is generated in synchronism with the operation of the recording medium (2) (see col. 6, l. 22-27 in combination with col. 5, l. 13-18 and 24-28).

D1 does not explicitly show write control means for writing signal-processed data into said storage means based on said first clock and read control means for reading out the data stored in said storage means based on said second clock. The board considers such control means to be a necessary and thus implicit feature whenever read/write processes into a memory occur. An indication that a read/write control is actually present in the device of Fig. 1 of D1 is given by the control routine performed by the microprocessor 10 based on the filling degree indicator Vg2 shown in Fig. 4. The appellant did not contest the finding that read/write control means are implicit in the device shown in D1.

The decoder circuit of D1 is also, in the board's view, suitable for a shock-proof system. The requirement for a decoder to be suitable for a shock-proof system is the existence of a buffer memory of a sufficient size (col. 12, l. 23-27 of the application in suit as published). In D1 it is considered to be "essential that the storage capacity is selected to be adequate to compensate for the resulting fluctuations in the amount of information stored", col. 15, lines 45 to 48. Taking into account the considerations under point 2.2 above, the board concludes that the teaching of D1 implies a sufficiently large memory size also to compensate for shock induced fluctuations.

3.2 The prima facie difference between the decoder according to claim 1 and the decoder known from D1 lies in the second clock explicitly being a stabilized clock, independent of and different from the first clock.

The board considers that the presence of two separate clock generators 8 and 9 shown in Fig. 1 of D1, although they are not described as being different and independent, would suggest to the skilled person that the generated clock rates are different from each other. Furthermore, it would be part of the general knowledge of the skilled person that a decoder/encoder of the type shown in Fig. 1 of D1, as indeed most electronic devices, requires a stabilized system clock which is used as a reference clock for subsystems. Clock generator 9 supplies a signal having a frequency related to the scanning speed of the record carrier (col. 6, l. 25-27) for the input and output buffer memories 6 and 11 respectively, whereas clock generator 8 supplies the remaining subsystems, implying a stabilized system clock. These two findings were not contested by the appellant.

The reasons for the independence of the two clocks was stated by the appellant to be to allow for compensation of shock induced slip movements of the medium with respect to the medium carrier. Such movements would, because of the first clock generator being in synchronism with the operation of the medium, require a clock independent of the system clock which controls the second clock.

In this respect, the appellant argued that, according to his understanding, the scanning speed in D1 (col. 6,

lines 25-27) on which the first clock was based did not relate to the rotation of the medium but rather to that of the medium carrier. The rotation of the latter would, however, be related to the system clock. Thus, the first and second clock were not truly independent of each other.

Notwithstanding the problems of claim interpretation discussed at point 2 above, and for the sake of argument assuming that the "recording medium" is to be understood as being a "disk recording medium" and the "operation" as "reading the groove information from the disk", the scanning speed from which the first clock signal derives (col. 6, lines 25-27) must be understood as "the speed with which the record carrier 2 is moved past the read/write head" (col. 5, lines 25-28), and is thus indicative of the movements of the recording medium including possible slip motion of the same with respect to a medium carrier, and thus independent of the system clock on which the turntable speed depends.

3.3 The appellant furthermore argued that D1 was concerned with a recording and reading system working at a lower bit rate than the designed bit rate without detriment to the information density on the recording medium, and not only did not address shock-proof systems at all but actually discounted the subject-matter in the discussion of D2 (see col. 3, l. 6-17 of D1), which relates to shock-proof systems.

On a proper reading of the above passage of D1, it becomes clear however that D2 is discounted only because its object, the reduction of the susceptibility of the servo systems to shock, is different; however,

the physical means to achieve this object, the provision of different reading and recording speeds by means of a buffer memory, are identical to those of D1. The skilled person who was aware of this similarity would not have been discouraged from considering the system of D1 for application in a shock-proof system. If he did so he would arrive at the subject-matter of claim 1.

Therefore, the subject-matter of claim 1 of the main request is obvious, Article 56 EPC, in the light of the disclosure of D1.

3.4 The above considerations apply, mutatis mutandis, to the subject-matter of claim 7, with the encoder known from D1 comprising a buffer memory (6 in Fig. 1) and first and second signal processing means (5a and 50 in Fig. 5a). All other features correspond to those already discussed above under points 3.1 to 3.3.

Therefore, the subject-matter of claim 7 of the main request is obvious, Article 56 EPC, in the light of the disclosure of D1.

3.5 The subject-matter of claims 1 and 7 being obvious in the light of the disclosure of D1, the main request is not allowable.

4. *Inventive step, auxiliary request (Article 56 EPC)*

4.1 The additional features of claim 1 according to the auxiliary request relate to read and write pointers used by the read and write control means for designating the read out address and the data write

address of the storage means, and to the write control means restarting the operation of reading out data from the recording medium if the data storage amount of the storage means becomes lower than a predetermined data amount at a certain time instant, thus ensuring that the storage means fill factor does not fall below a minimum value.

The use of read and write pointers for designating the data read address and the data write address of a memory is a standard procedure in the art, and cannot justify an inventive step. This finding was not contested by the appellant.

The specific feature ensuring that the storage means fill factor does not fall below a minimum value is not explicitly discussed in D1 in connection with the decoder. This feature is, however, discussed in connection with the encoder, where the recording process is stopped once the storage means fill factor falls below a minimum value (see step S6 in Fig. 2) in order to ensure an uninterrupted data stream at the recording head.

With regard to the decoder claimed in claim 1, it would have been obvious for the skilled person to apply an equivalent feature in order to ensure an uninterrupted data stream at the decoder output. This is self-evidently necessary in audio or video applications where the interruption of the data stream at the output of an audio/video player would be unacceptable.

Therefore, the subject-matter of claim 1 is rendered obvious, Article 56 EPC, by the teaching of D1.

4.2 D1 furthermore shows the recording being started once the fill factor goes beyond a given fill factor (Fig. 2, step S3).

Therefore, the subject-matter of claim 7 is rendered obvious, Article 56 EPC by the teaching of D1.

4.3 The subject-matter of claims 1 and 7 being obvious in the light of the disclosure of D1, the auxiliary request is not allowable.

5. As there is no allowable request it follows that the appeal must be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar The Chairman

D. Magliano A. S. Clelland