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D E C I S I O N
of 12 May 2005

Case Number: T 0781/01 - 3.5.3

Application Number: 92108517.1

Publication Number: 0514866

IPC: H04J 3/07

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Title of invention:
Stuff bit synchronization system

Patentee:
MITSUBISHI DENKI KABUSHIKI KAISHA

Opponent:
ALCATEL

Headword:
Stuff bit synchronization system/MITSUBISHI

Relevant legal provisions:
EPC Art. 100(b), 111(1), 83
EPC R. 65(1)

Keyword:
"Admissibility of the appeal (yes)"
"Disclosure - sufficiency (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0781/01 - 3.5.3

D E C I S I O N
of the Technical Board of Appeal 3.5.3
of 12 May 2005

Appellant: (Proprietor of the patent)	MITSUBISHI DENKI KABUSHIKI KAISHA 2-2-3, Marunouchi Chiyoda-ku Tokyo (JP)
Representative:	Gleiter, H. Dipl.-Phys. Dr. Pfenning, Meinig & Partner GbR Mozartstrasse 17 D-80336 München (DE)
Respondent: (Opponent)	ALCATEL 54, rue de la Boétie F-75008 Paris (FR)
Representative:	Knecht, Ulrich Karl, Dipl.-Ing. Alcatel Intellectual Property Department Stuttgart D-70430 Stuttgart (DE)
Decision under appeal:	**Decision of the opposition division of the European Patent Office posted 14 May 2001 revoking European patent No. 0514866 pursuant to Article 102(1) EPC.**

Composition of the Board:

Chairman: A. S. Clelland
Members: F. van der Voort
R. T. Menapace

Summary of Facts and Submissions

I. This appeal is against the decision of the opposition division revoking European patent No. 0 514 866 on the ground that the patent did not disclose the invention in a manner sufficiently clear and complete for it to be carried out by a person skilled in the art (Article 100(b) EPC).

II. In addition to the ground pursuant to Article 100(b) EPC opposition was filed on the ground that the subject-matter of each of the claims lacked novelty (Article 100(a) EPC). In support of this ground the opponent referred, *inter alia*, to the following documents:

D1: EP 0 422 443 A (cited in the patent specification); and

D3: R. Graf, Modern Dictionary of Electronics, 5th edition, 1978, page 294.

III. The proprietor (appellant) lodged an appeal against this decision and requested that the decision be set aside and the patent maintained as granted. Oral proceedings were conditionally requested. In the statement of grounds of appeal the appellant essentially argued as follows:

D1 constituted the closest prior art and the subject-matter of claim 1 was distinguished from the disclosure of D1 in that in accordance with the claim a variable frequency divider was provided. The disclosure was sufficient to enable the person skilled in the art to

carry out the invention as claimed. Further, the appellant argued that starting out from the disclosure of D1, it could easily be seen how to employ a variable frequency divider in the bit stuffing method described in D1. The claims were therefore considered to be sufficiently clear and enabling, despite some admittedly misleading wording in the patent specification, which could be corrected if necessary.

IV. In response to the statement of grounds of appeal, the respondent (opponent) requested that the appeal be dismissed. The respondent argued that the appellant's arguments for sufficiency were solely based on the disclosure of an unrelated patent document, i.e. D1, which was not relevant to the question of sufficiency of disclosure, since patent documents normally did not belong to the common general knowledge and D1 was not referred to in the application as filed. The appeal was thus not adequately substantiated and therefore inadmissible. In addition, the respondent contested in substance the appellant's arguments and concluded that, if the board were to admit the appeal, it was not allowable. Oral proceedings were conditionally requested.

V. The appellant in reply argued that the statement of grounds was sufficiently detailed for the appeal to be admissible. A detailed explanation of the manner of operation of the invention was given. Amended description pages were filed in order to bring the specification in conformity with claim 1.

VI. In his reply, the respondent argued that the amendments made to the description violated Article 123(2) EPC.

Further arguments were presented in support of the alleged insufficiency of disclosure. The respondent requested that the appeal be dismissed (main request). By way of a first auxiliary request he requested that, if the board were minded not to consider inventive step, the case be remitted to the first instance for further examination as to novelty and, if necessary, inventive step. Further, by way of a second auxiliary request, the respondent requested that a question on the relationship between objections of insufficiency and inventive step in opposition proceedings be referred to the Enlarged Board of Appeal.

VII. The parties were summoned by the board to oral proceedings. In a communication accompanying the summons, the board drew attention to issues to be discussed at the oral proceedings and gave a preliminary opinion on the question of the admissibility of the appeal.

VIII. Oral proceedings were held on 12 May 2005 during which the appellant requested that the decision under appeal be set aside and the patent be maintained either as granted (main request) or with an amended set of claims as filed with letter dated 30 March 2005 in preparation for the oral proceedings (auxiliary request). The respondent requested that the appeal be dismissed (main request) or that the case be remitted to the department of first instance for further prosecution (first auxiliary request) or that a question (see point VI above) be referred to the Enlarged Board of Appeal (second auxiliary request).

At the end of the oral proceedings the board's decision was announced.

IX. Claim 1 as granted reads as follows:

"A stuff bit synchronization system, comprising:

a) a transmitter for transmitting a digital signal, said transmitter comprising:

i) transmitter-side memory means (20) for temporarily holding the digital signal to be transmitted;

ii) transmitter-side reading means (22,26) for controlling the reading of the transmitter-side memory means (20) so that a bit stored in the transmitter-side memory means (20) is read twice to provide a stuff bit that is inserted into the digital signal which is read from the transmitter-side memory means (20) in parallel and transmitted by the transmitter;

b) a transmission path for the digital signal; and

c) a receiver for receiving the digital signal and removing the stuff bit from the digital signal,

characterized in that

the transmitter-side reading means (22,26) comprises a variable frequency divider."

Claim 6 as granted reads as follows:

"A stuff bit synchronization system, comprising:

a) a transmitter for transmitting a digital signal, said transmitter comprising:

i) a transmitter-side memory means (20) for temporarily holding the digital signal to be transmitted;

ii) a transmitter-side reading means (22,26) for controlling the reading of the transmitter-side memory means (20) so that a bit stored in the transmitter-side memory means (20) is not read to provide a stuff bit that is deleted from the digital signal which is read from the transmitter-side memory means (20) in parallel and transmitted by the transmitter;

b) a transmission path for the digital signal; and

c) a receiver for receiving the digital signal and inserting in the stuff bit from the digital signal,

characterized in that

the transmitter-side reading means comprises a variable frequency divider."

The claims of the appellant's first auxiliary request and the question to be referred to the Enlarged Board of Appeal in accordance with the respondent's second auxiliary request are not relevant to the present decision. Accordingly, neither is reproduced here.

Reasons for the Decision

1. *Admissibility*

1.1 The respondent argued that the appellant's argument, set out in the written statement of grounds of appeal, as to why the patent specification was sufficient was

solely based on the content of an unrelated patent document (D1) which was not relevant to the question of sufficiency of disclosure, since patent documents normally did not belong to the common general knowledge and the patent document was not referred to in the application as filed. The appeal was accordingly not adequately substantiated.

1.2 In the board's view, however, the statement of grounds of appeal sufficiently specifies the legal and factual reasons on which the case for setting aside the decision is based; it is argued that the opposition ground pursuant to Article 100(b) EPC does not prejudice the maintenance of the patent as granted, since a person skilled in the art, starting from D1, would not need any specific information in order to be able to implement the variable frequency divider of the stuff bit synchronization system according to the patent in suit. The question of whether D1, or at least those parts of it referred to by the appellant in the statement of grounds of appeal, can be taken to represent the common general knowledge in the art cannot be answered in the negative solely on the basis of the fact that D1 is a patent document; a consideration of its contents is required. Such consideration however forms part of the examination of the allowability of the appeal, which presupposes the admissibility of the appeal (Article 110(1) EPC).

1.3 The written statement is thus held to constitute grounds of appeal in accordance with Article 108 EPC.

1.4 The other requirements for the admissibility of the present appeal were not contested by the respondent and the board is satisfied that they are met.

1.5 The appeal is accordingly held admissible (Rule 65(1) EPC).

2. *Sufficiency of disclosure*

2.1 The opposition division held that, even in the light of the common general knowledge in the art, the person skilled in the art would not be able to implement the variable frequency divider performing the required operations and, in particular, the manner in which such a variable frequency divider allows positive or negative bit stuffing (see the reasons for the decision, point 3).

2.2 The board is however of the view that the patent discloses the stuff bit synchronization system, in particular the variable frequency divider and its operation in relation to the bit stuffing, in a manner which is sufficiently clear and complete for it to be carried out by a person skilled in the art. The reasons are as follows.

2.3 Figure 1 of the patent specification shows a block diagram of a preferred embodiment of the transmitter section of the stuff bit synchronization system. A serial digital input signal "g" is sequentially written into a buffer memory 20 by means of a write clock signal "h" (column 6, lines 11 to 15). The data is sequentially read out, however as a parallel output signal "i" consisting of N parallel bits (column 6,

lines 15 to 19 and 45 to 47 and Figure 2). The read operation is controlled by an actuating or read clock signal which is generated by a reading means 22 synchronized with a clock source 28 and which, hence, has a fixed read clock period (column 6, lines 6 to 8 and 19 to 24 and Figure 2, top line). The memory addresses which are read out during each read clock period are determined by a memory address outputted by the reading means 22. If the outputted memory address is n, N memory addresses are read out in parallel, namely memory addresses n up to and including n+(N-1) (column 6, lines 39 to 47). In the next clock period, the outputted memory address is incremented by N to n+N so that the N subsequent memory addresses, i.e. from n+N up to (n+N)+(N-1) = n+2N-1, are read out (column 6, lines 48 to 55). Since the read clock signal is synchronized with the clock source 28, the same applies to the output signal "i".

The above-described operation of reading out a memory under the control of a sequentially incrementing memory address outputted by a reading means was well-known before the priority date of the patent in suit and was not the issue under debate between the parties during the opposition and appeal proceedings.

2.4 Further, it was common ground between the parties that the technique of bit stuffing for bit synchronizing an input signal with an output signal, in which the bit rate of the input signal slightly deviates from or slightly varies in time with respect to that of a reference clock signal used for reading out the output signal from a buffer memory in which the input signal is temporarily stored, was known before the priority

date. In order to achieve synchronization, the phases of the write and read clock signals applied to the buffer memory are compared and, dependent on the result, a stuff bit inserted into the output signal during the reading out of the memory in the next clock period (see column 1, lines 11 to 17 of the patent specification). The block diagram of Figure 6 of the patent specification illustrates a prior art transmitter section of a conventional stuff bit synchronization system for serial input and serial output signals.

2.5 In the synchronization system according to the patent in suit, the bit stuffing is accomplished by modifying the address generated by the reading means 22. The address modification is controlled by a read control means 26 and is dependent on a phase comparison of the write and read clock signals at a phase comparator 24 (column 5, line 54 to column 6, line 6). If the insertion of a stuff bit is necessary, the memory address n+N-1 (instead of n+N, see point 2.3) is outputted by the reading means 22, resulting in the reading out of the N memory addresses from n+N-1 up to n+N-1+(N-1) = n+2N-2 in the next clock period (see Figure 3 and column 7, lines 26 to 39). Memory address n+N-1 is thereby read out twice; the extra bit serves as a stuff bit in the synchronized parallel output signal "i".

2.6 So-called "negative stuffing" is also described; instead of the insertion of at least one stuff bit (positive stuffing), in order to achieve synchronization it may be necessary to skip at least one stored bit on reading out the buffer memory (negative stuffing). This is accomplished by having the

read control means 26 controlling the reading means 22 to output memory address (n+N)+1 for the next clock period (column 7, line 55 to column 8, line 18 and Figure 4). The skipped bit may be a pre-inserted stuff bit (column 11, lines 4 to 9).

2.7 In relation to the bit stuffing operation and the corresponding memory address outputted by the reading means 22 the patent specification refers to the use of a "variable frequency divider of the reading means" (column 6, lines 40 and 41, column 7, lines 43 and 44). In particular, at column 6, lines 24 to 27, it is stated that "*In the normal state in which no stuff bit is inserted, the variable frequency divider of the reading means 22 generates up to N clock pulses for each clock period.*" and, similarly, at column 7, lines 42 to 45, it is stated that "*If there is no insertion of a stuff bit in the clock period following the next clock period, the output of the variable frequency divider of the reading means is incremented by N ...*". However, with respect to the negative stuffing it is stated at column 8, lines 8 to 10 that "*For example, if one input signal bit is cancelled, the increment of the variable divider is set at (N+1) by the read control means 26*" and at column 8, lines 18 to 21, "*When negative stuffing is no longer desired immediately after negative stuffing is carried out, the output of the variable divider is incremented by N to (n+2N+1)*".

2.8 From these statements, it follows that the number of pulses, i.e. sum of pulses, generated by the variable frequency divider within one read clock period is to be set differently, depending on whether negative or no

bit stuffing is required, as is determined by the read control means 26. If no stuffing is required, the frequency divider generates N pulses per read clock period, whereas for negative stuffing by one bit the frequency divider generates N+1 pulses. It also follows that for positive stuffing with one stuff bit (see point 2.5 above) the frequency divider would generate N-1 pulses.

Further, from the timing charts of Figures 2 to 4 it follows that the memory address outputted by the reading means for the next read clock period is obtained by incrementing the previous address by N if no stuffing is required, N-1 in case of positive stuffing, and N+1 in case of negative stuffing.

Hence, in each case the sum of pulses generated by the variable frequency divider per read clock period is equal to the increment in the memory address. For example, if the sum of pulses is equal to 8, the increment will also be 8, corresponding to no stuffing with N = 8 parallel bits, whereas if the sum is 7 or 9, the increment will be 7 (positive stuffing) or 9 (negative stuffing), respectively.

2.9 However, the patent specification does not provide information about how the different numbers of pulses are generated by the variable frequency divider and how their sums are obtained in order to be used as the desired increment in the memory address outputted by the reading means.

2.10 In the board's view, however, a person skilled in the art would without undue difficulty be able to fill in

this lacuna on the basis of his common general knowledge. More specifically, as follows from D3, which is a prior art dictionary of electronics, a "frequency divider" may be defined as "*A counter which has a gating structure added that provides an output pulse after a specified number of input pulses are received*". The board therefore interprets the term "variable frequency divider" as a counter which has a gating structure added which provides an output pulse after a variably selectable number of input pulses is received. This interpretation was not contested by the respondent.

Applying this interpretation to the system of the patent in suit implies that for the example given above, if the clock source generates, e.g., 7x8x9 = 504 pulses within one read clock period, the gating structure of the variable frequency divider would have to be set by the read control means 26 such that it provides one output pulse after either 8x9 = 72, 7x9 = 63 or 7x8 = 56 input pulses are received from the clock source 28, thereby generating a total of 7, 8 or 9 pulses per read clock period in order to achieve the required sum of pulses for positive stuffing, no stuffing or negative stuffing, respectively. The variable frequency divider thereby effectively divides the clock frequency rate of clock source 28 by 72, 63 or 56, respectively. All that is demanded of the skilled person is accordingly the use of a counter for obtaining the actual sum of pulses, namely by counting the pulses outputted by the variable frequency divider. The board considers this knowledge as being part of the common general knowledge of a person skilled in the art at the priority date, since digital pulse counters were well-known at that time.

2.11 It follows that the patent specification, taking into account the common general knowledge of a person skilled in the art, provides a sufficiently clear teaching to enable the skilled person to implement the bit synchronization system.

2.12 The board would further comment that claims 1 and 6 define neither the purpose nor the technical effect to be achieved by the variable frequency divider. Nor is any connection to the other parts of the system specified. The skilled person would thus have no difficulty in merely providing the reading means with a variable frequency divider in accordance with these claims.

2.13 The ground for opposition pursuant to Article 100(b) EPC only refers to the patent; nevertheless, in the board's view it must also be taken to mean that the application as originally filed must disclose the invention as claimed in a manner sufficiently clear and complete for it to be carried out by a person skilled in the art at its priority(/filing) date as required by Article 83 EPC. Since all of the above references to the patent specification, except for a number of obvious corrections of reference signs, were already contained in the application as filed, the board is satisfied that the application as filed met the requirements of Article 83 EPC.

2.14 The board notes, as acknowledged by the appellant, that some statements in the description appear to be incorrect, inconsistent and/or in contradiction with the wording of the claims. In view of the reasons set

out above (see points 2.3 to 2.10) these matters are however not so serious as to give rise to further objections of insufficiency. Further, although inconsistencies between parts of the description on the one hand and the claims on the other hand may render the claims unclear and/or not supported by the description, thereby contravening the requirements of Article 84 EPC, this is not a ground for opposition (cf. Article 100 EPC).

2.15 The board therefore concludes that the opposition ground according to Article 100(b) EPC does not prejudice the maintenance of the patent as granted.

3. Since the ground of opposition under Article 100(a) EPC was not discussed in the impugned decision, which is solely based on Article 100(b) EPC, the board considers it appropriate to remit the case to the department of first instance pursuant to Article 111(1) EPC for further prosecution, in order not to deprive the parties of an examination of the further opposition ground (Article 100(a) EPC) by two instances. The board notes that at the oral proceedings the appellant submitted that he preferred this course of action rather than have the board consider the matter by virtue of its right to exercise any power within the competence of the opposition division, Article 111(1) EPC.

The board accordingly accedes to the respondent's first auxiliary request so that it has not proved necessary to consider the respondent's second auxiliary request concerning the referral of a question to the Enlarged Board of Appeal (see point VI above).

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance for further prosecution.

The Registrar: The Chairman:

D. Magliano A. S. Clelland