BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [ ] To Chairmen
(D) [X] No distribution

D E C I S I O N
of 22 October 2004

Case Number: T 0760/01 - 3.5.3

Application Number: 99307100.0

Publication Number: 0987861

IPC: H04L 12/56

Language of the proceedings: EN

Title of invention:
Flexible telecommunications switching network

Applicant:
LUCENT TECHNOLOGIES INC.

Opponent:
-

Headword:
Flexible telecommunications switching network/LUCENT

Relevant legal provisions:
EPC Art. 52, 56

Keyword:
"Inventive step - no"

Decisions cited:
-

Catchword:
-

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0760/01 - 3.5.3

D E C I S I O N
of the Technical Board of Appeal 3.5.3
of 22 October 2004

Appellant: LUCENT TECHNOLOGIES INC.
600 Mountain Avenue
Murray Hill
New Jersey 07974-0636 (US)

Representative: Watts, Christopher Malcolm Kelway, Dr.
Lucent Technologies (UK) Ltd.
5 Mornington Road
Woodford Green
Essex IG8 0TU (GB)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 1 February 2001 refusing European application No. 99307100.0 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: A. S. Clelland
Members: D. H. Rees
R. Moufang

Summary of Facts and Submissions

I. This is an appeal from the decision of the examining division to refuse the European patent application number 99 307 100.0, publication number 0 987 861, dispatched on 1 February 2001. The reason given for the refusal was that the claimed subject-matter did not involve an inventive step with respect to the disclosure of

D1: EP-A-0 854 613.

II. Notice of appeal was filed and the fee paid on 6 March 2001. New claims 1 to 26 were submitted with a statement setting out the grounds for the appeal on 4 June 2001.

III. In a communication the board gave its preliminary view that the subject-matter of the newly-filed claims still did not involve an inventive step with respect to D1 and the common general knowledge of the person skilled in the art. To illustrate the common general knowledge the board cited extracts from a textbook

D6: D.L. Cannon et al., "Understanding Microprocessors", Texas Instruments, Dallas, Texas, 1979, page iv, "Preface", and pages 1-28 and 1-29, "System design trends".

IV. The appellant responded in a letter dated 17 May 2004 with further arguments.

V. The appellant requests that the decision of the examining division be cancelled in its entirety and a patent granted on the basis of the following text:

Claims: 1 to 26 submitted with the grounds of appeal;
Description: pages 1 to 29 as originally filed,
insert on page 2 received 25 August 2000;
Drawings: sheets 1 to 19 as originally filed.

VI. The single independent claim 1 reads as follows:
"A telecommunications switching network fabric element (100) comprising:
a plurality of input buffers (101, 102), each for receiving an input bit stream;
means connected to the input buffers by a multi-byte bus for receiving a plurality of bytes; and
a plurality of output buffers (111, 112), each for transmitting an output bit stream;
wherein difference [sic] ones of at least one of said input bit streams and said output bit streams comprise data transmitted in different protocols;
characterised in that:
said means for receiving comprises a microprocessor (120) comprising an internal memory (201, 211);
the microprocessor is programmed to perform switching and protocol conversion functions; and
said microprocessor is programmed to convert between protocols within signals of one input stream and protocols within signals of one output stream, while switching said signals of said one input stream to said signals of said one output stream."

Reasons for the Decision

1. The claims filed with the statement setting out the grounds of the appeal are based on the claims of the original application, with minor amendments for clarity. In particular the present independent claim is based on a combination of originally filed claims 1 to 3. The board therefore concludes that Article 123(2) EPC is satisfied.

2. Document D1 discloses the following features specified in the current independent claim:
A telecommunications switching network fabric element (D1, page 2, lines 3 to 5) comprising:
a plurality of input buffers (figure 2, elements 104 and 110; page 6, lines 10 to 19; figure 3A, receive FIFOs 302; page 25, lines 12 to 18; figure 8C, data buffers 826), each for receiving an input bit stream;
means (figure 2, "EPSM" 210) connected to the input buffers by a multi-byte bus for receiving a plurality of bytes (figure 2, buses HSB 206 and PCI 222; page 5, lines 16 to 18 and 39 to 41); and
a plurality of output buffers (figure 2, 104 and 110; page 6, lines 10 to 19; figure 3A, transmit FIFOs 304; page 25, lines 12 to 18; figure 8C, data buffers 826), each for transmitting an output bit stream;
wherein different ones of at least one of said input bit streams and said output bit streams comprise data transmitted in different protocols (page 2, lines 46 and 47; page 4, lines 18 to 42, 54 and 55).

3. The remaining features of claim 1 specify that a microprocessor having an internal memory carries out switching and protocol conversion functions between

input and output streams. In D1 these functions are carried out by a combination of an Ethernet Packet Switch Manager "EPSM" (figure 2, 210) together with a microcontroller "CPU" 230. The EPSM is associated with a memory 212.

4. The board considers that it has been a general trend in the last thirty years to replace specialised hardware by standard integrated components and in particular by microprocessors. Moreover the flexibility of microprocessor solutions was well known at the priority date of the present application, giving the additional advantage that a single device might be used for several functions simply by amending the microprocessor software, where previous solutions had required devices whose hardware had to be tailored to the separate functions. It belonged to the standard considerations of the skilled person in the field to weigh up whether newly available microprocessors could replace specialised hardware in existing systems (particularly in the light of the ever increasing processing speed and ever decreasing cost of microprocessors over this period), and no inventive step can be seen in simply claiming the replacement of such specialised hardware by a microprocessor. That this was general knowledge is witnessed by textbook D6, in particular the third paragraph of the preface, and the whole of the section "System design trends" on pages 1-28 and 1-29.

5. Frequently of course the development process of replacing specialised hardware by a microprocessor may have thrown up problems which required an inventive step in their solution, but no such problem and solution has been identified or claimed in this case.

6. In the appellant's final submission it was argued that D1 did not, in fact, disclose protocol conversion, but merely speed conversion (appellant's letter of 17 May 2004, page 2, lines 18 and 19, and page 3, lines 16 to 20). The board is not convinced by this argument. The document D1 distinguishes between differences in protocols and simple differences in speed, and clearly envisages conversion of protocols, even though the preferred embodiment only relates to the respective Ethernet protocols for two different speeds - see D1, page 4, lines 39 to 42, in particular "The 'A' type ports and networks operate at a different network protocol and/or speed than the 'B' type ports and networks." The present claimed subject-matter does not limit the protocols converted in any way, nor does it specify any particular technical feature to effect the conversion, beyond it being carried out by a microprocessor.

7. The appellant further argued in this submission (page 2, lines 20 to 31) that the statement in D1 that the EPSM is "not limited to any particular physical or logical implementation" (D1, page 5, lines 19 to 21), implied that the authors of D1 did not contemplate its implementation as software in a microprocessor. This in turn was an indication that such an implementation was not obvious. In the opinion of the board the failure to include an alternative explicitly cannot be seen as positive evidence that any alternative would involve an inventive step. Thus the board is also not persuaded by this argument.

8. It was further argued (page 2, lines 32 to 36) that even if the skilled person were to consider integrating CPU 230 and EPSM 210, it would be a substantial further step to consider the further integration of the blocks 202, 226 and 220, these being the Ethernet ports and an interface device (D1, figure 2). However there is no subject-matter in the present claim 1 specifying that the equivalent features in the present application are integrated into the microprocessor. To the extent that equivalent features can be identified in the claim (e.g. the input buffers), they are merely specified to be part of the "fabric element". Figure 1 of the application shows this to be a module consisting of a number of separate components; in particular, the buffers are not shown as part of the microprocessor. Be that as it may, the trend to integrate functions into a microprocessor was a general one; the skilled person would have implemented as many functions into the microprocessor as were consonant with the performance requirements and possibilities of the system.

9. Hence the subject-matter of claim 1 is obvious to the skilled person in the light of the disclosure of D1 and the common general knowledge in the art, and the text of the appellant's sole request does not satisfy the requirements of Articles 52 and 56 EPC.

10. There being no other requests, it follows that the appeal must be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

D. Magliano A. S. Clelland