BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS
BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE
CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [X] To Chairmen
(D) [ ] No distribution

D E C I S I O N
of 31 March 2004

Case Number: T 0536/01 - 3.4.3

Application Number: 93910567.2

Publication Number: 0641485

IPC: H01L 21/306

Language of the proceedings: EN

Title of invention:
Membrane dielectric isolation IC fabrication

Applicant:
LEEDY, Glenn J.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (denied)"

Decisions cited:
-

Catchword:
-

Case Number: T 0536/01 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 31 March 2004

Appellant: LEEDY, Glenn J.
1061 E. Mountain Drive
Santa Barbara, CA 93108 (US)

Representative: Wombwell, Francis
Potts, Kerr & Co.
15, Hamilton Square
Birkenhead
Merseyside CH41 6BR (GB)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 11 December 2000 refusing European application No. 93910567.2 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: V. L. P. Frank
M. B. Günzel

Summary of Facts and Submissions

I. The appeal lies from the decision of the Examining Division dated 11 December 2000 refusing the European patent application No. 93 910 567.2. The ground for the refusal was *inter alia* that the method of making a dielectrically isolated integrated circuit according to independent claim 1 was not new (Article 52(1) and 54 EPC) over the disclosure of the prior art document:

D1: US-A-4 070 230

II. The appellant (applicant) lodged an appeal against the above decision on 8 February 2001, paying the appeal fee on 10 February 2001. The statement setting out the grounds of appeal was filed on 10 April 2001.

III. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of claims 1 to 35 submitted with the statement of grounds of appeal. The appellant submitted furthermore a declaration of Dr Alain Harrus.

IV. In response to a communication of the Board under Article 11(1) RPBA accompanying the summons to oral proceedings the appellant submitted with his letter dated 27 January 2004 amended pages of the description and two sets of claims 1 to 35 marked, respectively, as "Corrected copy claims filed on 16/02/00" and "Auxiliary amended claims". In the letter the appellant's representative further stated in respect of the "auxiliary amended claims" that "The applicant also herewith submits a newly amended set of claims wherein claim 1 has been amended, and requests that this

auxiliary amended set of claims be considered as **the preferred claims** for the purpose of the current proceedings" (emphasis added by the Board).

In this letter, the appellant withdrew his previous request for oral proceedings and requested that the procedure be continued in writing and that a written decision be issued based upon his written submissions.

The wording of claim 1 according to the appellant's requests is as follows:

Corrected copy of claims filed on 16 February 2000, hereinafter Request A:

"1. A method of making a dielectrically isolated integrated circuit comprising the steps of:

providing a substrate (10) having a principal surface;

forming an etch barrier layer (12) in the substrate parallel to the principal surface;

forming, as part of the integrated circuit, semiconductor devices (24, 26, 28) on the principal surface;

after forming the semiconductor devices, depositing a low stress insulating membrane (20) over the semiconductor devices, the low stress insulating membrane forming the primary structural means of the integrated circuit; and

etching away to the etch barrier layer (12) a portion (11) of the substrate from a backside of the substrate opposite the principal surface."

Auxiliary amended claims, hereinafter Request B:

"1. A method of making a dielectrically isolated integrated circuit comprising the steps of:

providing a substrate (10) having a principal surface;

forming an etch barrier layer (12) in the substrate parallel to the principal surface;

forming, as part of the integrated circuit, semiconductor devices (24, 26, 28) on the principal surface;

after forming the semiconductor devices, depositing a stress controlled silicon dioxide membrane (20), that is, capable of withstanding standard high-temperature semiconductor processing steps of approximately 400°C over the semiconductor devices, wherein the stress of the membrane is less than 8×10^8 dynes/cm^2 and wherein the stress of the membrane is tensile; and

removing beneath the etch barrier layer (12) a substantial portion (11) of the substrate from a backside of the substrate opposite the principal surface while retaining the structural integrity of the integrated circuit."

V. The oral proceedings as scheduled were held before the Board on 31 March 2004 in the absence of the appellant and a decision to dismiss the appeal for the reasons which follow was announced at the end of the proceedings.

VI. The arguments of the appellant can be summarized as follows:

The closest state of the art is represented by document D1, which discloses a dielectrically isolated integrated circuit in which a synthetic material, preferably polyamide 1-10 µm thick, is applied over the finished circuit wafer. However, all organic films cure with a high tensile stress (typically 2 x 10^9 dynes/cm^2 or greater). A honeycombed structure is therefore left on the backside of the wafer such that every individual circuit fabricated is supported at its edge by a silicon wall. These walls are required to counteract the stress of the organic film which would cause the circuit, once cut from the wafer, to curl or crack.

In contrast, the stress-controlled silicon dioxide membrane used in the present invention renders it unnecessary to buttress each IC with a support ring, but only a support ring at the edge of the wafer is used for ease of handling during fabrication. The key distinction of the present invention is, therefore, the use of a stress-controlled silicon dioxide membrane having a tensile stress less than 8 x 10^8 dynes/cm^2 over the semiconductor devices. According to the declaration of Dr Harrus, such a stress-controlled membrane could not have been formed at the time of the invention of document D1, since at that time deposition equipments with dual frequency power supplies were not available.

Reasons for the Decision

1. The appeal is admissible.

2. *Appellant's requests A and B*

As pointed out in item V above, the appellant stated in respect of the "Auxiliary amended claims" (Request B), "The applicant also herewith submits a newly amended set of claims wherein claim 1 has been amended, and requests that this **auxiliary** amended set of claims be considered as **the preferred claims** for the purpose of the current proceedings" (emphasis added by the Board).

It seems, therefore, that the appellant preferred the grant of a patent on the basis of the claims of Request B, i.e. the "Auxiliary amended claims". However, identifying a set of claims as "auxiliary" usually indicates that another request has precedence in the order of preference in which the requests should be dealt with by the Board.

In the present case, since claim 1 of Request B includes all the features of claim 1 of Request A, the following consideration of inventive step of claim 1 of Request B applies to claim 1 of Request A as well. The above ambiguity in the order in which the requests are to be considered is, therefore, irrelevant.

3. *Claim 1 - Request B, Inventive step*

3.1 The application in suit relates to a method for producing integrated circuits (IC) on and in flexible dielectric membranes. This approach is usually referred

to as dielectric isolation (DI) and consists in completely isolating an individual IC from other circuits. The DI fabrication method reduces the complexity of producing a completely isolated IC device when compared to the traditional approach of forming ICs in a bulk semiconductor substrate, avoiding the problems of parasitic transistor effects between adjoining circuits, capacitive coupling and substrate current leakage (cf. the application in suit, page 1, lines 9 to 11 and 21 to 34; page 3, lines 4 to 13; page 4, line 31 to page 5, line 1).

3.2 It is common ground that document D1 represents the closest state of the art. This document discloses as prior art a DI method in which a few micron thick silicon dioxide layer is formed over a monocrystalline silicon wafer. The silicon wafer is then thinned by etching it from the side opposite to the one on which the dielectric layer was formed.

Document D1, however, discloses further that this prior art technique has the disadvantage of a relatively high outlay for the application of the silicon dioxide dielectric layer. The aim of document D1 is therefore to provide a method for assembling integrated circuits wherein the production outlay is reduced. To this effect a synthetic dielectric layer, e.g. a layer of polyimide, instead of a silicon dioxide layer is used, since the starting material for the synthetic layer can be spun onto the wafer in a manner similar to that employed for applying a conventional photolithographic layer, i.e. a simpler and less expensive process than the deposition of a silicon dioxide layer (cf. D1,

column 1, lines 17 to 24 and 31 to 34; column 2, lines 9 to 13; column 3, lines 21 to 30 and 38 to 42).

The DI process, as described in document D1, consists therefore in forming the desired ICs 8 in the surface of a silicon wafer 1 and covering the whole surface with a dielectric isolation layer 9. A suitable etch-stop layer is formed in the substrate and the wafer's rear surface is removed by conventional etching up to the etch-stop layer. The thinning of the silicon wafer is done so that a wall 1' of the initial wafer's material is left standing perimetrically about the peripheral edge portions of each IC forming a frame serving as support for the dielectric insulating layer 9. The components which are thus formed bear each an integrated semiconductor circuit and can easily be separated from one another in the form of chips (cf. column 3, lines 57 to 65; column 4, lines 49 to 55; column 5, lines 7 to 15 and 34 to 45; Figures 1 to 4).

3.3 The method according to claim 1 differs, therefore, from the method disclosed in document D1 in that a stress controlled silicon dioxide membrane having a tensile stress of less than 8×10^{8} dynes/cm^{2} is used instead of a synthetic organic layer as the dielectric isolation layer.

3.4 According to the application in suit, a dielectric isolation layer made of silicon dioxide allows the processing of the semiconductor device at temperatures of about 400°C. Moreover, a stress controlled silicon dioxide layer reduces the stress applied to the semiconductor membrane and, therefore, the occurrence of cracks or curling of the device (cf. the application

in suit, page 1A, lines 3 to 9 and the paragraph bridging pages 3 and 4 of the appellant's letter of 27 February 2004).

The objective technical problem addressed by the application in suit having regard to document D1 as the closest state of the art is, therefore, to provide a fabrication method for obtaining high temperature, mechanically durable, free standing integrated circuits (cf. the application in suit, page 2, lines 4 to 11).

3.5 However, as disclosed in document D1, silicon dioxide dielectric isolation layers have already been used in the state of the art for obtaining dielectrically isolated integrated circuits. The reason given in document D1 for departing from this fabrication method is the high cost associated with the deposition of a silicon dioxide layer. It thus follows from document D1 that if the cost of production was not a consideration then silicon dioxide was a suitable material for the dielectric isolation layer.

Confronted with the problem of cracks or curls in the semiconductor device due to the stress of the silicon dioxide layer, the skilled person would look for a deposition method that allows the control of this property.

3.6 According to the declaration of Dr A. Harrus, the company Novellus introduced in 1988 a dual-RF PECVD deposition system which provided for the first time a mechanism to control the stress of the deposited films. In this system stress is controlled by varying the energy ratio of high and low frequency RF sources. The

resulting low-energy ion implantation occurring during deposition causes a change in the intrinsic film stress from tensile to compressive, increasing film density, and improving the chemical reactions (cf. point 6 of the declaration).

Mr Leedy, the inventor of the present application, contacted Dr Harrus in 1990 about the feasibility of producing very low tensile stress films (cf. ibid, point 9).

At that time, Novellus had completed a substantial body of work regarding stress control of thin films. This work suggested in theory that, by controlling deposition parameters (principally the ratio of high frequency RF energy to low frequency RF energy) the film stress could be controlled anywhere along a line passing through zero and extending from about 5×10^9 dynes/cm^2 compressive stress to 3×10^9 dynes/cm^2 tensile stress (cf. ibid, point 10).

3.7 It follows from the declaration of Dr Harrus that at least in 1990, i.e. before 8 April 1992, the priority date of the application in suit, a deposition method allowing the control of the stress of deposited films was available to the public in general, and to the skilled person in particular. The use of a generally available method for the purpose for which it has been developed does not, however, involve an inventive step.

The Board concludes therefore, that the skilled person would have applied the deposition method developed by Dr Harrus at Novellus for depositing a silicon dioxide layer having a tensile stress of less than 8×10^8

dynes/cm^2 in the fabrication method disclosed in document D1.

3.8 The appellant has argued that the application in suit renders it unnecessary to buttress each IC of the wafer with a support ring or "wall" as disclosed in document D1 and that only a support ring at the edge of the wafer is used for ease of handling during fabrication.

The Board, however, cannot follow this argument, since claim 1 specifies that a "*substantial portion*" of the wafer beneath the etch barrier is removed from the backside of the substrate while retaining the structural integrity of the integrated circuit. As can be recognized in Figure 3 of document D1 most of the substrate's material is removed beneath each integrated circuit. As the expression "*a substantial portion*" has no well defined quantitative meaning, the Board comes to the conclusion that in the method disclosed in document D1 also a "*substantial portion*" of the substrate is removed, since only a minor portion of the substrate remains as a frame surrounding each IC.

4. For these reasons, it is the judgment of the Board that the method according to claim 1 of request B does not involve an inventive step in the sense of Article 56 EPC.

As already mentioned in point 2, the reasoning on inventive step is also applicable to the method according to request A. This request fails, therefore, for the same reasons.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

D. Meyfarth R. K. Shukla