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D E C I S I O N
of 28 November 2001

Case Number: T 0492/01 - 3.5.1

Application Number: 98308800.6

Publication Number: 0954191

IPC: H04Q 7/32

Language of the proceedings: EN

Title of invention:
Adaptive digital radio communication system

Applicant:
LUCENT TECHNOLOGIES INC.

Opponent:
-

Headword:
Adaptive digital radio system/LUCENT

Relevant legal provisions:
EPC Art. 54(3), 56

Keyword:
"Inventive step (no)"

Decisions cited:
T 1133/98

Catchword:
-

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Case Number: T 0492/01 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 28 November 2001

Appellant: LUCENT TECHNOLOGIES INC.
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Representative: Buckley, Christopher Simon Thirsk
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 7 December 2000 refusing European patent application No. 98 308 800.6 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: S. V. Steinbrener
Members: A. S. Clelland
H. Preglau

Summary of Facts and Submissions

I. This appeal is against the decision of the examining division to refuse application No. 98 308 800.6 on the ground that independent claims 1, 8 and 11 lacked novelty having regard to the disclosure of the following document:

D1: WO-A-97 48188.

Document D1 is a PCT application published after the priority date of the present application but having an earlier date of filing and designating many of the same contracting states as the application; as the requirements of Article 158(2) EPC have been fulfilled, D1 falls within the field specified by Articles 54(3) and 56 EPC as relevant to novelty but not inventive step.

II. The examining division also expressed the view that a further document was relevant to inventive step;

D2: US-A-5 655 003.

III. The appellant (applicant) lodged an appeal against this decision and paid the prescribed fee. Together with the subsequently filed statement of grounds, revised claims of a main and auxiliary request were filed. It was argued that these revised claims were both novel and inventive having regard to the cited prior art.

IV. In a communication the Board expressed its preliminary opinion that the independent claims of both requests lacked an inventive step having regard to the common general knowledge in the art, that the independent

claims of the main request lacked novelty having regard to the disclosure of D1 and that the independent claims of the auxiliary request lacked an inventive step having regard to the disclosure of D2 and the following document:

D3: WO-A-95 17077.

D3 had been cited by the examining division. The Board also drew attention to the common general knowledge as exemplified by an extract from the following textbook:

D4: Cowan and Grant "Adaptive Filters", Prentice-Hall, Englewood Cliffs, NJ, 1985, pages 258 to 261.

The appellant was summoned to oral proceedings.

V. In response to the summons revised sets of claims of a main and auxiliary request were filed. It was argued that the prior art did not make use of an FPGA device which included system performance measurement and optimisation circuitry which could be reconfigured.

VI. Shortly before the oral proceedings the appellant, in a fax communication, stated that a representative was unable to attend the oral proceedings and requested that the proceedings should continue, taking into account the latest main and auxiliary requests and the accompanying comments. The oral proceedings were held on 28 November 2001.

VII. Claim 1 of the main request reads as follows:

"A method of receiving radio communication signals,

CHARACTERIZED BY the steps of:

receiving radio communication signals using receive circuitry (124) having an architecture fully implemented in at least one programmable device (203) formed by at least one Field Programmable Gate Array, FPGA, device, comprising a source decoder, channel decoder and digital demodulator as part of receive circuitry, and a system performance measurement and optimization circuit;

reconfiguring said source decoder, channel decoder and/or digital demodulator within the at least one programmable logic device (203) to change said architecture of said receive circuitry (124), where said architecture change modifies at least one of the channel symbol rate, occupied bandwidth, modulation technique, or multiple access technique for said receive circuitry (124) to receive said radio communications signals; and

measuring the signal quality of said radio communication signal, said architecture change of said receive circuitry (124) being based upon the results of said signal quality measurement."

Claim 9 of the main request is an independent claim to a method of transmitting radio communication signals and comprising, *mutatis mutandis*, the same features as claim 1.

Claim 14 of the main request is an independent claim to a radio transceiver and reads as follows:

"A radio transceiver CHARACTERIZED BY:

at least one programmable logic device (203) configured to fully implement a particular architecture for said radio transceiver (200) and formed by at least

one Field Programmable Gate Array, FPGA, device and comprising a transmit chain (128) formed as a source encoder (102), channel encoder (103) and digital modulator (104) and a receive chain (124) formed as a source decoder (108), channel decoder (107) and digital demodulator (106), and comprising a system performance measurement and optimization circuit (110) for reconfiguring said transmit and receive chain."

VIII. Claim 1 of the auxiliary request reads as follows:

"A method of receiving radio communication signals, CHARACTERIZED BY the steps of:

receiving radio communications signals using receive circuitry (124) having an architecture fully implemented in at least one programmable device (203) formed by at least one Field Programmable Gate Array, FPGA, device, comprising a source decoder, channel decoder and digital demodulator as part of receive circuitry, and a system performance measurement and optimization circuit; and

reconfiguring said source decoder, channel decoder and/or digital demodulator within the at least one programmable logic device (203) to change said architecture of said receive circuitry (124), where said architecture change modifies at least one of the channel symbol rate, occupied bandwidth, modulation technique, or multiple access technique for said receive circuitry (124) to receive said radio communications signals, wherein said reconfiguring is based on measurements of one of at least the average signal-to-noise ratio (SNR) at the input of a Digital Demodulator circuit, the channel symbol error rate (Ps) at the output of a Channel Decoder, and the bit error rate (BER) at the output of a Source Decoder."

Claim 6 of the auxiliary request is an independent claim to a method of transmitting radio communication signals and comprising, *mutatis mutandis*, the same features as claim 1.

Claim 11 of the auxiliary request is an independent claim to a radio transceiver and reads as follows:

"A radio transceiver CHARACTERIZED BY:
at least one programmable logic device (203) configured to fully implement a particular architecture for said radio transceiver (200) and formed by at least one Field Programmable Gate Array, FPGA, device and comprising a transmit chain (128) formed as a source encoder (102), channel encoder (103) and digital modulator (104) and a receive chain (124) formed as a source decoder (108), channel decoder (107) and digital demodulator (106) and a system performance measurement and optimization circuit (110) for reconfiguring said transmit and receive chain; wherein said reconfiguring is based on measurements of one of at least the average signal-to-noise ratio (SNR) at the input of a Digital Demodulator circuit, the channel symbol error rate (P_s) at the output of a Channel Decoder, and the bit error rate (BER) at the output of a Source Decoder."

IX. At the end of the oral proceedings, which were held in the absence of the appellant's representative, the Board's decision was announced by the Chairman.

Reasons for the Decision

1. *Basis of Decision*

Although the appellant did not attend the oral proceedings before the Board and therefore has not had an opportunity to comment on the argumentation in the present decision concerning one of the features of the invention as claimed (i.e. the use of a Field Programmable Gate Array), the Board is satisfied that Article 113(1) EPC has been complied with under the circumstances of the present case (see this Board's decision T 1133/98, not published, relating to a closely analogous situation).

2. *Technical background to the application*

2.1 The advent of digital signal processing devices has given rise to so-called "software radio" in which, as stated in the application, see the "Background to the Invention", "all of the baseband receiver functions are performed digitally, typically utilizing a digital signal processor or a general purpose processor, in which the processor executes program instructions to perform the baseband processing functions. As such, software radio takes the received radio signal... and recovers the channel symbol bits".

2.2 The application implicitly acknowledges that such devices were well known at the claimed priority date. Software radio is said in the application to permit different modes to be emulated in cellular telephony, for example both the US AMPS analog standard and a digital standard such as TDMA, used in the European GSM system. A disadvantage of known software radio technology is however said to be that computational speed is limited so that it is impractical for standards having high channel data rates such as wideband CDMA (W-CDMA).

2.3 It is observed in passing that this alleged limitation did not in fact exist at the claimed priority date. D2 shows an example of a software radio which supports W-CDMA; reference is directed to column 1, lines 50 to 64, and column 4, lines 8 to 24. D3 moreover refers at page 14, lines 18 to 25 to the receive path of an adaptive omni-modal radio apparatus capable of demodulating "broad band" CDMA signals, which the Board understands to be W-CDMA signals.

2.4 A further problem is said to arise from the nature of cellular systems, which are prone to many kinds of RF impairment such as shadowing, Rayleigh fading and multipath. Schemes to overcome these problems are said to reduce bandwidth. Although not explicitly stated the Board assumes that the implication is that the alleged low bandwidth of known digital radios is thereby reduced further.

2.5 The solution to these problems is said to lie in the use of a Programmable Logic Device (PLD) for digital signal processing. The appellant has not contested that the use of programmable logic devices in digital circuitry in general and the use of programmable signal processors in adaptive digital receivers in particular were common general knowledge at the claimed priority date. The originally filed application identifies various classes of programmable logic device and states in the "Summary of the Invention" that this is "a general term representing a family of programmable logic devices; examples of this family are a Programmable Array Logic (PAL), a complex PLD (CPLD) and a Field Programmable Gate Array (FPGA)". No details of such devices are given. The Board takes this to mean that at the claimed priority date the skilled person

would have been aware of such devices and their properties, so that no detailed description was necessary. D1, albeit in the Article 54(3) EPC field, states before the claimed priority date that FPGA devices were regarded as "conventional" (page 6, lines 3 to 5). Reference is directed to D3 at page 9, lines 14 to 16, which gives an example of a multi-mode software radio implemented on "a single VLSI chip or on a set of VLSI chips making up a chipset". It is stated at page 10, lines 3 to 7 that the circuit "can be adjusted by the user, or automatically under stored program control, to transfer information over at least two different radio communications networks". In the Board's view the VLSI chip or chipset used in D3 can be regarded as constitutiing a PAL device.

3. *Inventive step (main request)*

3.1 The only objection arising in the present case is based on Articles 52(1) and 56 EPC.

Independent claim 14, an apparatus claim, will be considered first. This claim is directed to a radio transceiver having the following features:

(a) at least one programmable logic device configured to fully implement a particular architecture for said radio transceiver;

(b) formed by at least one Field Programmable Gate Array, FPGA, device;

(c) a transmit chain formed as a source encoder, channel encoder and digital modulator;

(d) a receive chain formed as a source decoder, channel decoder and digital demodulator; and

(e) a system performance and optimization circuit for reconfiguring said transmit and receive chain.

3.2 In the Board’s view the single most relevant document is D2 which, referring to Figure 2 and column 2, line 35 to column 3, line 18, discloses a digital transceiver making use of programmable processors 205, 206 and 215, 216 under the control of a stored program source 225. In the Board's view a "programmable processor" is an example of a "programmable logic device". For a digital transmitter and receiver it is necessary to provide source and channel encoders and decoders and associated modulators/demodulators, see column 2, lines 39 to 44. Thus, features (a), (c), and (d) of claim 14 are either directly disclosed or implicit in D2.

3.3 As regards feature (e), it is observed that the broad wording of claim 14 is not limited to any specific form of "system performance and optimization". Although claims 1 and 9 refer to measuring signal quality and changing the architecture based on this measurement, no such limitation is present in claim 14. The feature appears to the Board to be much wider in scope than changing the architecture in response to a signal quality measurement; it equally embraces reconfiguration in response to signal format as disclosed in connection with the stored program source 225 in D2 and illustrated in the flow charts of Figures 4 to 8, where in each case a frequency is first tuned and then an estimate made as to whether signal strength is adequate. The Board accordingly concludes

that feature (e) is known from D2.

3.4 But even if additional stress were to be put on the word "optimization" in feature (e), it appears to the Board that an essential function of any transceiver is to optimise transmission and reception conditions; at column 7, lines 18 to 27, D2 states that stored program instructions may be used in the context of a "radio port", i.e. a transceiver, to control "many procedures", the examples given being system synchronization, FEC, forward access channel information and data collection. It is also noted that D2 makes repeated references in column 3 to error control for different standards, whilst at column 4, lines 18 to 21 reference is made to "grades of service" with differing bit error rates. The Board accordingly concludes that even on a narrow reading of feature (e) it is present in D2.

3.5 The only distinguishing feature in claim 14 with respect to the transceiver known from D2 according lies in feature (b), the use specifically of an FPGA device. It is however evident from paragraph 2.5 above that at the claimed priority date the skilled person was aware of the use of programmable logic devices for digital radio. The published application discusses such devices at page 3, lines 48 to 55 and refers to them as a "family" including inter alia the FPGA device. Neither the application nor D2 discusses the properties of PLD devices, implying that they were well-known in the art at the claimed priority date. Nor does the application give any particular advantage arising from the use of a FPGA device. The Board accordingly concludes that the skilled person would without the exercise of invention have appreciated that the programmable logic device

embodying the programmable processor of D2 could be implemented by a programmable gate array device, the FPGA being one of the well-known array devices at his disposal.

3.6 A distinction emphasised by the appellant in the submissions to the examining division was that the application uses "at least one programmable logic device" whereas D2 uses programmable processors 205, 206 and 215, 216. Although the examining division seems to have accepted that the former is a piece of specially configured hardware and the latter is a software-driven general purpose processor, it is not clear to the Board that any meaningful distinction exists between a "programmable logic device" and a "programmable processor". But even if a distinction were for the sake of argument to be made - say between an ASIC and a general purpose processor - the former merely performs in hardware what the latter performs in software, albeit somewhat faster, a fact well known to the skilled person. The skilled person, faced with the problem of the lack of sufficient speed of a general purpose processor would therefore have appreciated that speed could be increased by the use of a programmable logic device in the form of an ASIC. Thus, even on a narrower reading of the expression "programmable logic device" than the plain meaning of the words, objection of lack of inventive step still arises.

3.7 The subject-matter of claim 14 of the main request accordingly lacks an inventive step.

3.8 Claims 1 and 9 of the main request are respectively directed to a method of receiving and a method of transmitting radio communication signals, both claims

being based on the features of claim 14 and additionally limited by measuring the quality of the signal and changing the architecture to modify at least one of channel symbol rate, occupied bandwidth, modulation technique, or multiple access technique. As noted at point 3.4 above, a function of any transceiver is to optimise transmission and reception conditions, which implies the need to provide appropriate means of optimisation. As also noted, D2 makes repeated references in column 3 to error control for different standards, and at column 4, lines 18 to 21 to "grades of service" with differing bit error rates. Finally, D4 shows that it was common general knowledge at the claimed priority date to provide adaptive equalization using a programmable signal processor (see in particular page 261, first paragraph).

3.9 The Board accordingly considers that the skilled person, faced with the problem of optimising transmission and reception for time-varying radio channel conditions (see page 2, lines 25 to 27 of the published application) would without the exercise of invention have made use of the programmable properties of the D2 device to optimise operation. The Board therefore concludes that the subject-matter of claims 1 and 9 of the main request also lacks an inventive step.

4. *Inventive step (auxiliary request)*

4.1 Turning now to claim 11 of the auxiliary request, an independent apparatus claim, this differs from corresponding claim 14 of the main request in including the following feature:

(f) reconfiguration is based on measurements of one of

at least the average signal-to-noise ratio at the input of a Digital Demodulator circuit, the channel symbol error rate at the output of a Channel Decoder and the bit error rate at the output of a Source Decoder.

4.2 As noted at point 3.4 above, the optimisation of reception conditions is a function of any transceiver and is known per se from D2, which explicitly provides error control.

4.3 The subject-matter of claim 11 of the auxiliary request accordingly lacks an inventive step.

4.4 Claim 1 and 6 of the auxiliary request are respectively directed to a method of receiving and a method of transmitting radio communication signals, based on the subject-matter of claim 11 and therefore open to the same objection of lack of inventive step.

5. There being no further requests, it follows that the appeal must be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Kiehl S. V. Steinbrener