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**D E C I S I O N**  
**of 8 November 2002**

**Case Number:** T 0122/01 - 3.5.1

**Application Number:** 93304279.8

**Publication Number:** 0574177

**IPC:** G06F 1/32

**Language of the proceedings:** EN

**Title of invention:**

Method and apparatus for changing processor clock rate

**Patentee:**

TEXAS INSTRUMENTS INCORPORATED

**Opponent:**

Spandern, Uwe

**Headword:**

Processor clock rate/TEXAS INSTRUMENTS

**Relevant legal provisions:**

EPC Art. 56

**Keyword:**

"Inventive step (yes after amendment)"

**Decisions cited:**

T 0536/88

**Catchword:**

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Case Number: T 0122/01 - 3.5.1

**D E C I S I O N**  
**of the Technical Board of Appeal 3.5.1**  
**of 8 November 2002**

**Appellant:** Spandern, Uwe  
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**Decision under appeal:** Decision of the Opposition Division of the  
European Patent Office posted 15 November 2000  
rejecting the opposition filed against European  
patent No. 0 574 177 pursuant to Article 102(2)  
EPC.

**Composition of the Board:**

**Chairman:** S. V. Steinbrener  
**Members:** R. S. Wibergh  
E. Lachacinski

## Summary of Facts and Submissions

I. This is an appeal against the decision of the Opposition Division to reject the opposition against European Patent No. 0 574 177.

II. The appellant (opponent) opposed the patent on the grounds that the invention was not new or did not involve an inventive step (Article 100(a) EPC). Among the documents cited in the notice of opposition or introduced later in the proceedings are:

**D1:** English translation of JP-A-3-278210

**D4:** English translation of JP-A-61-156459.

The description of the patent furthermore refers to

**D0:** EP-A-0 426 410.

These documents were again referred to by the parties and the Board in the present appeal proceedings.

III. According to the impugned decision, D1, regarded as the closest prior art document, did not render the invention obvious, nor did any other cited document or combination of documents.

IV. In a communication pursuant to Article 11(2) of the Rules of Procedure of the Boards of Appeal it was considered that the subject-matter of claim 1 as granted might be obvious in view of a combination of D4 and D1.

V. By letter dated 7 October 2002 the respondent filed claims according to seven new requests and a statement by a technical expert.

- VI. Oral proceedings before the Board were held on 8 November 2002.

The appellant pointed out that he had not received the respondent's letter dated 7 October 2002 until 25 October 2002. Since the letter contained in particular a complex, fifteen pages long statement he had difficulties in preparing himself properly for the oral proceedings in the short time available to him. He would, however, not request postponement of the oral proceedings for this reason.

The Chairman regretted the fact that the delay had been caused by the EPO. It appeared that most pages of the respondent's original letter had disappeared in connection with a scanning operation for converting the letter into electronic form. When the mistake had been discovered the Board's registry had asked the respondent to send a copy of the letter which was subsequently transmitted to the appellant.

- VII. During the oral proceedings the respondent filed new claims 1 to 11 and an adapted description according to a single new request.

Claim 1 read as follows:

"A method for changing a processor clock rate, wherein the processor (24) operates on a system bus, comprising:

detecting (12,16,20) a request to change the processor clock rate;

changing (26) the processor clock rate in response to the request to change the processor clock rate; and

instructing the processor (24) to relinquish control of the bus in response to the request to change the processor clock rate; the method including:

detecting (18) completion of a bus cycle, when

there is a bus cycle to be completed, and wherein the processor relinquishes control of the bus in response to detecting completion of said bus cycle, and

waiting (28,30) for the processor (24) to lock onto the changed processor clock rate; and instructing the processor (24) to resume activity on the bus".

Independent claim 7 was directed to a corresponding circuit.

- VIII. The appellant requested that the decision under appeal be set aside and that the patent be revoked.
- IX. The respondent requested that the decision under appeal be set aside and that the patent be maintained as amended on the basis of the claims and the pages of the description submitted at the oral proceedings before the Board.
- X. At the end of the oral proceedings the Chairman announced the Board's decision.

**Reasons for the Decision**

1. *Amendments*

Method claim 1 now includes the feature that the processor relinquishes control of the bus *in response to detecting completion of a bus cycle*, an amendment which brings the method claims into line with the apparatus claims. Otherwise new claim 1 corresponds to claim 4 as granted. Similarly, independent apparatus claim 7 (previously 8) corresponds to claim 11 as granted. The appellant has raised no objections under Article 123 EPC against the new claims and the Board sees no reasons for doing so either.

The description has been brought into conformity with the new claims mainly by excluding the embodiments in which the processor clock is stopped rather than being reduced to a non-zero value.

2. *Construction of claim 1*

An important term in the claims is "to relinquish control" of the bus, which must be attributed a particular meaning. It is mentioned in the description that certain processors have inputs which cause them to "relinquish" the bus, such as a "backoff" pin or AHOLD or HOLD inputs (column 4, l. 11 to 16). The description more frequently refers to "floating" the bus and the Board takes the expressions "relinquish" and "float" to be synonymous in the present context. "Processors 'float' the bus by entering into a state in which they no longer have control of the system bus" (column 5, l. 44,45); "Processor 24 floats the bus by releasing control of the bus. This is performed by entering into a high-z or low-z state in which processor 24 is effectively neither driving nor receiving signals from the bus" (column 6, lines 42 to 45). These quotations make it clear that floating or relinquishing the bus involves isolating the processor from the bus, eg by tri-stating.

3. *The closest prior art*

3.1 The Board regards D4 as the closest prior art document D4 discloses two bus control circuits, one (11) on the CPU side and one (12) on a clock generator side (see Figure 1). In normal operation (page 2, paragraph 4 to page 3, paragraph 3) a peripheral unit gains access to the bus by transmitting a bus request signal BR which is applied to the control circuit 11. When it has been detected that any on-going bus cycle has been completed (by means of the signal

BEND) a bus grant signal BG is returned to the peripheral. The peripheral replies by issuing a bus grant acknowledge signal BGACK which is applied to a tri-state bus inverter 26 in the bus controller 11 (page 15, lines 13 to 15).

Besides the normal mode there is a low power consumption mode in which the CPU clock is stopped. In this mode a signal BR transmitted by a peripheral is not applied to the bus control 11 but to the bus control on the clock generator side 12. The reason for the change is that, in prior devices, "in the low power consumption mode, the clock input is stopped... and its operation is stopped, and thus, the above-described operation can not be effected" (page 3, paragraph 4). This indicates that the bus controller 11 is inoperable to some degree when the CPU has been stopped. The bus controller 12 outputs a bus grant signal BG after a predetermined delay conforming to the bus protocol (Figure 2). At this point the peripheral will send a BGACK signal. The respondent has submitted that this signal is applied to the tri-state inverter, as in the normal mode. This is a crucial point of the interpretation of D4 because if the bus inverter 26 reacts to the BGACK by tri-stating its output, D4 cannot be regarded as disclosing that the processor is instructed to relinquish control of the bus *in response to the request to change the processor clock rate*, as required by claim 1. In the respondent's view the control is relinquished later, at the reception of a BGACK signal.

- 3.2 It is in favour of the respondent's reading of D4 that in Figure 1 the only signal which is shown to be applied to the tri-state inverter is BGACK. This is however not decisive since the drawing, which is schematic, cannot be assumed to show all circuit connections.

According to the description of D4 "the bus grant acknowledge signal is the signal which is received by the CPU to open the bus" (page 7, lines 12,13). Furthermore, "the bus control is set by the clock generator by opening the bus by the third clocked inverter in the bus control circuit on the CPU side" (page 15, lines 20 to 22). The "third clocked inverter" is the tri-state inverter on the bus, and thus both these passages seem to indicate that "to open the bus" has in D4 the meaning of setting the tri-state buffer 26 to its high-impedance state. "Opening" the bus would thus correspond to "relinquishing" the bus in the meaning of claim 1. As to *when* this is done, D4 states that "/when/ the control circuit on the clock generator side is selected, the bus is already opened", and "the CPU is constantly in the low power consumption mode when the bus control on the clock generator side is selected, and the bus is already opened at this moment" (page 7, lines 9,10; page 7, lines 15 to 17). In the Board's view these indications leave little room for any other interpretation than that the processor relinquishes control over ("opens") the bus (shortly) before entering the low power consumption mode. If so, there is no support for the reading that the bus is opened when - and if - a BGACK signal is received, as in the normal mode.

- 3.3 The respondent has argued that by "already opened" it is only meant that the bus is "available" in the sense that an extra bus controller 12 (which is the invention in D4) has been added to previous designs so as to enable peripherals to accede to the bus when the CPU is in the low power mode. "Opened" would thus simply refer to the presence of this new hardware. The Board cannot however accept this interpretation since "open" would then have two different meanings in D4, namely either signifying the presence of the bus control circuit 12 or referring to the action of the tri-state inverter



(cf the preceding paragraph). It is true that translations are always a potential source of error. Still, simply alleging that a certain term in D4 is ambiguous without evidence - eg a new, authorised translation of the document - is insufficient.

3.4 The Board therefore finds that D4 discloses, in the words of claim 1, a method for changing a processor clock rate, wherein the processor operates on a system bus, comprising detecting a request to change the processor clock rate (which is at least implicit), changing the processor clock rate (to zero) in response to this request, and instructing the processor to relinquish control of the bus in response to the request to change the processor clock rate. Whether this last feature is implicit in D4 or merely obvious from it may be debatable, but it seems in any case clear that the bus is only "opened" when necessary, ie when it has been decided to stop the processor.

4. The prior art mentioned in the patent

D0, the only prior art document to be identified in the description of the opposed patent, is automatically part of the opposition proceedings pursuant to decision T 536/88 (OJ EPO 1992,638).

5. *Inventive step*

5.1 D4 does not disclose the following features of claim 1:

- the processor relinquishing control of the bus in response to detecting the completion of a bus cycle,

- waiting for the processor to lock onto the changed processor clock rate, and

- instructing the processor to resume activity on the bus.

5.2 As to the first difference D4 discloses to open the bus provided that the current bus cycle has been terminated (as indicated by the signal BEND). This applies when a peripheral requests the bus in the normal mode. It is not disclosed that the same condition must be fulfilled when the processor opens the bus in connection with its being set to the low power mode, but this appears self-evident since otherwise data may be lost. The same problem and the same solution are moreover known as such from D1: "... a microcomputer enters a standby state synchronously with a bus cycle. This results in a microcomputer posing no problem in that it will not take place that the contents of an external memory are broken unexpectedly..." (page 6, paragraph 2). Therefore this feature appears to be an obvious addition to D4.

5.3 As to the second difference the fact that the processor is able to lock onto the changed processor clock implies that the processor is not stopped but the clock frequency is changed to some non-zero value. This represents a limitation compared with the patent as granted which covers both possibilities: changing the clock frequency as well as stopping the CPU.

The third difference indicates that the bus is relinquished only for the (brief) time it takes for the processor to lock on the new clock signal. In the described embodiment this time is about 1 ms (see column 7, lines 48 to 50).

These features are in the Board's opinion not obvious additions to the teaching of D4 for reasons to be given below.

- 5.4 In D4 the CPU is *stopped* for an *unspecified* time. It is therefore natural to regard the described method as one for deactivating a CPU. If the CPU of a microcomputer is stopped, possibly for considerable time, the problem mentioned in D4 that it cannot deal with bus requests from peripherals is immediately apparent. On the other hand, if the CPU clock frequency is merely reduced there is no such strong need to deal with bus requests received in the brief interval when the frequency is being changed since the loss of control will be almost instantaneous, at least from the user's point of view. Therefore, even if the skilled person would have considered D4 in the light of his knowledge that some processors can be stopped whereas others can only be slowed down (cf. the discussion about the Intel processors 80386 and 80286 in D0, bottom of column 14 respectively bottom of column 15), he may well have decided that the problem addressed in D4 was not relevant in case of a processor having its clock rate reduced and then directly resuming its activity. It is true that "real time power conservation", ie power reduction by clock frequency reduction during brief periods of inactivity (cf the patent-in-suit column 3, lines 11 to 26; column 4 lines 57,58) was known as such from D0 (eg column 5, lines 13 to 27). But there is no document on file which deals with the implication of real time power conservation on the bus control. Thus, even if the skilled person would for some reason read D4 in the light of D0 there is no suggestion that during the brief periods of inactivity involved in "real time power conservation" it would be advantageous to instruct the processor to relinquish control of the bus. In terms of the problem-solution approach, it

seems not possible without hindsight to derive a technical problem from D4 which is solved in D0 and leads to the invention. Nor does it appear that D0 would be a suitable starting document to which the teaching of D4 could be added.

5.5 The appellant has argued that a combination of D4 and D1 would lead to the invention. However, neither document even mentions the possibility that the CPU clock is slowed down instead of stopped. The appellant has pointed out that this feature was known as such. That is indeed the case, as discussed above. Still, D1 clearly cannot contribute to a solution to the question how to manage the bus in case the CPU clock frequency is reduced rather than stopped.

5.6 It follows that the method of claim 1 (and the circuit of claim 7) involves an inventive step.

## **Order**

### **For these reasons it is decided that:**

1. The decision under appeal is set aside.
2. The case is remitted to the first instance with the order to maintain the patent as amended in the following version:

**Description:** Column 1, lines 1 to 55 of the patent specification;  
pages 3 to 15 submitted at the oral proceedings on 8 November 2002;

**Claims:** 1 to 11 submitted at the oral proceedings on 8 November 2002;

**Drawing:** Figure 1 as granted.

The Registrar:

The Chairman:

M. Kiehl

S. Steinbrener