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D E C I S I O N
of 7 April 2003

Case Number: T 1180/00 - 3.5.2

Application Number: 94120465.3

Publication Number: 0661815

IPC: H03L 7/099

Language of the proceedings: EN

Title of invention:
Frequency Synthesizer

Applicant:
MITSUBISHI DENKI KABUSHIKI KAISHA

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - no"

Decisions cited:
-

Catchword:
-

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Case Number: T 1180/00 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 7 April 2003

Appellant: Mitsubishi Denki Kabushiki Kaisha
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 17 July 2000 refusing European patent application No. 94 120 465.3 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. G. O'Connell
Members: M. Ruggiu
B. J. Schachenmann

Summary of Facts and Submissions

I. The applicant appealed against the decision of the examining division refusing European patent application No. 94 120 465.3.

II. The reason for the refusal was essentially that the subject-matter of claim 1 was considered to lack an inventive step in view of prior art documents:

D1: US-A-3 973 209 and

D3: EP-A-0 277 726.

III. Oral proceedings were held before the board on 7 April 2003. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of claims filed with letter of 7 March 2003 in the form of a main and an auxiliary request.

IV. Independent claim 1 of the main request reads as follows:

"1. A frequency synthesizer arrangement with a direct digital synthesizer (22) being incorporated inside a phase-locked loop comprising:

(a) phase comparison means (1, 42, 56) which are adapted to detect a phase difference between a reference signal (A, J) and a comparison signal (B) and to output phase error information (C) having a sign and a magnitude of the phase error,

(b) a loop filter (2, 43, 55) which is adapted to generate loop control information (D) having a

sign and a magnitude for controlling the loop in accordance with the phase error information (C),

(c) the direct digital synthesizer (22) being adapted to the comparison signal (B) by employing a clock signal supplied from outside (32, 51) of the phase-locked loop and the loop control information (D) input as a phase incremental value (G); the direct digital synthesizer comprising:

(c-1) accumulator means (48) for receiving a phase incremental value (G) to produce phase information (H);

(c-2) memory means (49) for storing wave-form data addressed by the phase information (H);

(c-3) D/A converter means (50) for producing an analog value of the addressed wave-form data; and

(c-4) filter means (52) for filtering the analog values of the wave-form data to produce a comparison signal (B),

(d) phase increment correction means (31; 45, 46, 47) which are provided at the input side of the accumulator means (48) and adapted to receive the loop control information (D) and the correction information (K; E, F) comprising gain information (E) and offset information (F) from the outside of the loop, both provided by a CPU (47) outside of the frequency synthesizer to modify the loop characteristics to thereby produce the phase incremental value,

whereby an output synchronizing signal (I) which follows the frequency of the reference signal (A, J) is generated, the reference signal (A, J) being variable

over a broad range."

Claims 2 to 4 of the main request are dependent on claim 1.

V. Independent claim 1 of the auxiliary request reads as follows:

"1. A frequency synthesizer arrangement with a direct digital synthesizer (22) being incorporated inside a phase-locked loop comprising:

(a) phase comparison means (1, 42, 56) which are adapted to detect a phase difference between a reference signal (A, J) and a comparison signal (B) and to output phase error information (C) having a sign and a magnitude of the phase error,

(b) a loop filter (2, 43, 55) which is adapted to generate loop control information (D) having a sign and a magnitude for controlling the loop in accordance with the phase error information (C),

(c) the direct digital synthesizer (22) being adapted to the comparison signal (B) by employing a clock signal supplied from outside (32, 51) of the phase-locked loop and the loop control information (D) input as a phase incremental value (G); the direct digital synthesizer comprising:

(c-1) accumulator means (48) for receiving a phase incremental value (G) to produce phase information (H);

(c-2) memory means (49) for storing wave-form data addressed by the phase information (H);

(c-3) D/A converter means (50) for producing an

analog value of the addressed wave-form data; and

(c-4) filter means (52) for filtering the analog values of the wave-form data to produce a comparison signal (B),

(d) phase increment correction means (31; 45, 46, 47) which are provided at the input side of the accumulator means (48), and adapted to receive the loop control information (D) and the correction information (K; E, F) comprising gain information (E) and offset information (F) from the outside of the loop, both provided by a CPU (47) outside of the frequency synthesizer to modify the loop characteristics to thereby produce the phase incremental value, wherein the phase increment correction means comprise a multiplier (45) receiving the loop control information (D) and the gain information (E) and forming a product thereof, and an adder (46) arranged at the output side of the multiplier and receiving the offset information (F) and forming a sum of the offset information and the product which is output by the multiplier,

whereby an output synchronizing signal (I) which follows the frequency of the reference signal (A, J) is generated, the reference signal (A, J) being variable over a broad range."

Claims 2 to 4 of the auxiliary request are dependent on claim 1.

VI. The arguments of the appellant can be summarised as follows:

Document D1 disclosed an arrangement with a direct digital synthesizer incorporated inside a phase-locked loop comprising features (a), (b) and (c) as specified in claim 1 of the main and auxiliary requests. However, document D1 did not disclose phase increment correction means. In particular the purpose of the fixed register 16 shown in document D1 was to set a nominal frequency for the phase locked loop, not to provide a correction. Furthermore D1 did not mention any gain correction or multiplier.

Document D3 described a different kind of apparatus, namely an NCO (numerically controlled oscillator), and not a DDS (direct digital synthesizer) as in document D1. Thus, it would not be obvious to the skilled person to combine D3 with D1. Furthermore, D3 did not describe in any detail the loop bandwidth control unit 8 mentioned therein. In the arrangement described in D3, a multiplier 7 was disposed at the output side of an accumulator, before a phase comparator, and not at the input side of the accumulator as in the invention. Positioning the multiplier before the phase comparator, as in D3, resulted in increased jitter as compared to the invention, in which the multiplier was positioned downstream of the phase comparator. There was also no suggestion in the prior art that a multiplier receiving gain information and an adder receiving offset information should be positioned as specified in claim 1 of the auxiliary request.

Neither D1 nor D3, nor any of the other documents cited in the examination procedure, mentioned a CPU. The use of a CPU in the kind of apparatus to which the invention related was therefore not documented. Furthermore, the use of a CPU was not as common at the

priority date of the invention, as it was to become later. The description of the present application indicated that a setting switch or a CPU could be used to provide a set value for the gain information or the offset information. In the case of a setting switch, an operator provided intelligence in actuating the switch. When a CPU was used as specified in the claims, it also provided intelligence in setting the gain information and the offset information. The invention avoided uncoordinated information acting on the loop, which could result in increased jitter, by providing both the gain information and the offset information from a common CPU that processed both information signals.

Thus, a multiplicity of steps was necessary to arrive at the invention by way of a combination of D1 with D3, and some of these steps were undocumented, which showed that the invention involved an inventive step. Furthermore, there was no indication that the skilled person would, as opposed to could, arrive at the arrangement defined by the present claims.

Reasons for the Decision

1. The appeal is admissible.

2. The appellant agrees with the board that document D1 discloses a frequency synthesizer arrangement having features (a), (b) and (c) of claim 1 of either request. In particular, in the arrangement of D1, an incoming signal is coupled to an input of a phase comparator 10 which also receives, on another input, an output signal of the synthesizer. The output signal from the phase comparator is an analog signal which is low pass

filtered and converted to a digital signal by a low pass filter 102 and an analog-to-digital converter 11, respectively. The arrangement described in D1 furthermore includes a digital register 16 in which a number representing a base or nominal frequency is set from the outside of the phase-locked loop. An adder 15 adds the number in the register 16 to digital loop control information derived from the filtered and A/D converted output of the phase comparator 10. The result of the addition is transferred to the input of a digital accumulator 17, the output of which is used as an address to perform a table look-up in a read-only-memory to read out signal values approximating a sine wave. After digital-analog conversion and filtering of the signal values read out, an output signal is obtained which follows the frequency of the variable reference signal applied at the input of the phase comparator 10 and which is applied to the other input of the phase comparator 10.

The digital register 16 and the adder 15 mentioned in D1 are provided at the input side of the accumulator 17 to add an offset value, which is provided from outside the phase-locked loop, to the loop control information. The digital register 16 and adder 15 thus produce the effect of modifying the loop characteristics. In particular, they shift the follow-up range of the loop, which is the effect provided by the "offset information" specified in claim 1 of the present application. Thus, the board regards the digital register 16 and adder 15 of D1 as constituting phase increment correction means in the sense of the present invention.

3. The subject-matter of claim 1 of the main request

differs from the arrangement disclosed in D1 in that the phase increment correction means, which are provided at the input side of the accumulator means, are adapted to receive not only offset information but also gain information from the outside of the phase-locked loop, and that both the offset information and the gain information are provided by a CPU outside of the frequency synthesizer.

4. The subject-matter of claim 1 of the auxiliary request differs from the arrangement disclosed in D1, in addition to the differences found for the main request and identified above, also in that a multiplier is provided for receiving the loop control information and the gain information and forming a product thereof, and that an adder is arranged at the output side of the multiplier for receiving the offset information and forming a sum of the offset information and the product which is output by the multiplier.

5. Document D3 describes a digital phase-locked loop in which the bandwidth, and thus the breadth of the follow-up range of the loop is adjusted by means of a multiplier 7 operating to adjust the loop gain under the control of a loop bandwidth control unit 8. The multiplier 7 is positioned between the output of a digital accumulator 1, 4 and a first input of a phase detector latch 9 which samples the value C at the output of the multiplier 7 in response to a transition in a square wave F constituting a reference signal applied to a second input of the phase detector latch 9. The latter thereby provides a number representative of the phase error of the output signal of the digital accumulator with respect to said square wave. According to D3, the multiplier 7 preferably implements the

multiplication by shifting the number it receives from the digital accumulator 1, 4. Furthermore, the phase-locked loop of D3 comprises a frequency offset adder 3 which allows the centre frequency of the operation of the phase-locked loop to be adjusted at will and, to that effect, adds a centre frequency control word G from a centre frequency control unit 2 to loop control information E derived from the output of the phase detector latch 9.

6. Both documents D1 and D3 relate to phase-locked loops with digital accumulators, in which the follow-up range of the loop is shifted by digitally adding a number representing an offset value to the loop control information representing the phase error. Thus, the board considers that document D3 is so close to document D1 that it would be part of the state of the art taken into account by the designer of the frequency synthesizer arrangement disclosed in D1.

7. The problem of adjusting the breadth of the follow-up range of the phase-locked loop of D1, which is mentioned in the present application, is obvious to the skilled person in view of D3, which suggests adjusting the bandwidth and thus the breadth of the follow-up range by modifying the loop gain.

8. The preferred implementation described in D3 for adjusting the loop gain is digital and consists in shifting a number which represents in digital form the value of the phase error in the loop, so as to multiply this digital value under the control of a bandwith control unit. In the view of the board, the skilled person would tend to resort to this known digital implementation for providing adjustment of the loop

gain in the arrangement described in D1. Therefore, it would be obvious to the skilled person to insert a shift multiplier in the digital portion of the loop described in D1. The skilled person would not insert the shift multiplier between the output of the adder 15 and the input of the accumulator 17 of D1, because at that location the multiplier would shift multiply and thus significantly change the base or nominal frequency specified by the number in the digital register 16, which is clearly undesirable. However, it is apparent to the skilled person that the shift multiplier could appropriately be inserted at any position in the digital portion of the loop described in D1 where it would not change the base or nominal frequency of the loop. Thus, an obvious possibility for the skilled person would be to insert the shift multiplier at the input side of the adder 15, so that the adder would be arranged at the output side of the multiplier and form a sum of the offset information it receives from the fixed register and the product which is output by the multiplier.

9. Neither document D1 nor document D3 indicate precisely which source provides the offset information that is added to the loop control information. Furthermore D3 does not indicate precisely how the shift multiplier is controlled by the loop bandwidth control unit.

However, D1 indicates that the arrangement described there is useful in communications equipment and, in the judgement of the board, it is notorious, even if not documented, that at the priority date of the present application, i.e. in 1993, it was usual to control communications equipment by means of CPUs provided therein. It is also notorious that a CPU is a digital

device able to provide digital information to circuitry external thereto. Thus, the board considers that a CPU constitutes an obvious possibility for providing digital information, in particular gain and offset information, to the digital portion of a phase locked loop. In this respect, the board further observes that the present application discloses that the CPU provides the gain information and the offset information, but not that it processes this information.

10. Therefore, the board has come to the conclusion that, starting from the prior art disclosed in document D1, the skilled person would arrive in an obvious manner at the subject-matter of claim 1, in accordance with either the main or the auxiliary request, which thus cannot be considered as involving an inventive step in the sense of Article 56 EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

D. Sauter R. G. O'Connell