BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [ ] To Chairmen
(D) [X] No distribution

D E C I S I O N
of 29 January 2003

Case Number: T 1103/00 - 3.5.2

Application Number: 96929640.9

Publication Number: 0847625

IPC: H03K 19/08

Language of the proceedings: EN

Title of invention:
LOGIC CIRCUITS

Applicant:
TELEFONAKTIEBOLAGET L M ERICSSON (publ)

Opponent:
-

Headword:

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
-

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 1103/00 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 29 January 2003

Appellant: TELEFONAKTIEBOLAGET L M ERICSSON (publ)
126 25 Stockholm (SE)

Representative: Rosenquist, Per Olof
Bergenstrahle & Linvall AB
P.O. Box 17704
118 93 Stockholm (SE)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 7 April 2000 refusing European patent application No. 96 929 640.9 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: R. G. O'Connell
P. Mühlens

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division to refuse European patent application No. 96 929 640.9.

II. The reason given for the refusal was that the subject-matter of claims 1 and 9 lacked unity of invention within the meaning of Article 82 EPC, because the inverter shown in Figure 1 of the application (and claimed in claim 9) was obvious.

III. As filed the application contains nine claims. Claim 1 is worded as follows:

"A logic circuit having at least a first input terminal and at least a first output terminal, characterized in

- that it comprises at least a first and a second electron-wave Y-branch switch (2, 3), each having a source (S2, S3), a first drain (D2', D3'), a second drain (D2'', D3''), and at least a first gate (G2, G3) for switching a source current (I_{DD}) between the first and the second drain (D2', D3'; D2'', D3''),

- that the sources (S2, S3) of said first and second Y-branch switches (2,3) are adapted to be connected to a high voltage supply and a low voltage supply, respectively,

- that the first gates (G2, G3) of said first and second Y-branch switches (2,3) are interconnected, the interconnection point between said first gates (G2, G3) constituting said first input terminal,

- that the first drain (D2') of the first Y-branch switch (2) is connected to the second drain (D3'') of the second Y-branch switch (3), and

- that the second drain (D2'') of the first Y-branch switch (2) is connected to the first drain (D3') of the second Y-branch switch (3), the interconnection point between said second drain (D2'') of the first Y-branch switch (2) and said first drain (D3') of the second Y-branch switch (3) constituting said first output terminal."

Independent claim 5 is worded as follows:

"A logic circuit having at least one input terminal and one output terminal, characterized in

- that it comprises an electron-wave Y-branch switch (14) having a source (S14), a first drain (D14'), a second drain (D14''), and a gate (G14) constituting a first input terminal,

- that the first drain (D14') and the second drain (D14'') are adapted to be connected to a low voltage supply and a high voltage supply, respectively, and

- that the source (S14) constitutes said output terminal."

Independent claim 9 is worded as follows:

"A logic circuit having an input terminal and an output terminal, characterized in

- that it comprises an electron-wave Y-branch switch (1) having a source (S1), a first drain (D1'), a second drain (D1''), and a gate (G1) constituting said input terminal for switching a source current (I_{DD}) between the first and the second drain (D1', D1''),

- that the source (S1) is adapted to be connected to a high supply voltage (V_{DD}), and

- that the first drain (D1') in series with a first resistor (R1') and the second drain (D1'') in series with a second resistor (R1'') are adapted to be connected to a low supply voltage, the interconnection point between the second drain (D1'') and the second resistor (R1'') constituting said output terminal."

IV. Of the prior art documents referred to in the decision under appeal, the following remains relevant for the present decision:

D1: T. Palm et al.: "Quantum interference devices and field-effect transistors: A switch energy comparison", J. Appl. Phys. Vol. 74, No. 1, July 1993.

V. In the grounds of appeal the appellant argued that document D1 disclosed the design of a Y-branch switch, but did not suggest or disclose how to design a logic circuit using a Y-branch switch component. A Y-branch switch was a single component, so a person skilled in the art might use it to replace a single component of a known circuit, but it was not obvious without any hint at all to form a new circuit by replacing part of the circuitry with a Y-branch switch. There was no lack of unity, because all the claims related to logic circuits

in which a Y-branch switch was used as a switching element.

VI. In a communication the Board observed that the concept of current switching, also known as current steering, was notorious in the logic design art. It appeared to be obvious to make an inverter/buffer by arranging the known electron-wave switch to selectively direct the output current to respective load resistances at the output branches of the Y-branch switch as shown in Figure 1 of the present application. Document D1 compared and contrasted electron-wave Y-branch switches and FETs and referred to the potential of the former for added functionality. Given that a major application of FET devices was in the implementation of logic, it appeared that a person skilled in the art would appreciate the potential of electron-wave Y-branch switches as ultra-fast logic switches. All the claimed logic circuits appeared to be obvious analogues of standard transistor logic configurations, it being understood that electron-wave Y-branch switch devices were not direct substitutes for the FETs of a CMOS circuit, so that it was design by analogy taking account of the differences implied by the use of current steering devices.

VII. In reply the appellant pointed out that none of the cited prior art documents disclosed a logic circuit including an electron-wave Y-branch switch. D1 compared an electron-wave Y-branch switch with other devices including field effect transistors, resonant tunnel transistors and Aharonov-Bohm interferometers, and merely indicated that electron-wave Y-branch switches might be used for building large complex networks. Hindsight judgement should be avoided. The appellant

was willing to cancel claim 9 if necessary.

VIII. The appellant has made no explicit request, but it is implicit that the grant of a patent on the application as filed is sought as the main request, and the grant of a patent on the basis of claims 1 to 8 as filed is sought as an auxiliary request. There is no request for oral proceedings.

Reasons for the Decision

1. The appeal is admissible.

2. As acknowledged on page 1 of the present application, electron-wave Y-branch switches were already known in which by creating an electric field perpendicular to a branching waveguide electrons can be forced to enter the branch with the highest electrostatic potential. According to page 2, lines 9 and 10, the object of the invention is to design logic circuits using electron-wave Y-branch switches.

3. Document D1 compares and contrasts the properties of field effect transistors (FETs) with those of quantum interference devices (QIDs), exemplified by a Y-branch switch (shown in Figure 4 on page 690 of D1), a resonant tunnel transistor (RTT) and an Aharonov-Bohm interferometer. In the penultimate paragraph under the heading "VIII. Conclusions" on page 692 it is stated: "The Y-branch switch is a 1X2 device, i.e., rather than being an on/off device like the FET it switches a signal between two exits. Thus it too has a potential for added functionality."

4. The concept of current switching, also known as current steering, is notorious in the logic design art. Once electron-wave Y-branch switches became available, a person skilled in the art would immediately appreciate their potential as ultra-fast logic switches. It was, therefore, obvious to move on to design logic circuits exploiting them.

5. In the Board's communication, it was observed that the circuits to which claims 1 to 8 are directed appeared to be obvious analogues of standard transistor logic configurations, it being understood that electron-wave Y-branch switch devices were not direct substitutes for the FETs of a CMOS circuit, so that it was a design by analogy which took account of the differences implied by the use of current steering devices.

6. The clearest example of this design by analogy is provided by the logic circuit according to claim 5, which differs from an electron-wave Y-branch switch per se (such as shown in D1, Figure 4) only in that the so-called first and second drains are "adapted to be connected to a low voltage supply and a high voltage supply, respectively" and in that the so-called source constitutes the output terminal of the logic circuit. In other words, claim 5 covers an electron-wave Y-branch switch per se (since no other component is specified) "adapted" (in a manner which is not specified) to be connected as specified for use as a logic circuit (whose function is not specified).

7. In the judgement of the Board, it would be obvious to a person skilled in the art, stimulated by D1, to want to design an inverter or buffer circuit using an electron-wave Y-branch switch. It would be obvious to him that

the Y-branch switch had to be arranged so as to connect either the upper voltage supply or the lower voltage supply to the output in dependence on an input logic level voltage applied to the gate of the Y-switch. It would be obvious to him that one way in which he could try to do this would be to connect the branches of the Y to the upper voltage supply and the lower voltage supply, respectively, and the common part of the Y to the output. Proceeding along this obvious route, he would arrive at a logic circuit according to claim 5.

8. Therefore, the subject-matter of claim 5 of both the appellant's present requests does not involve an inventive step within the meaning of Article 56 EPC.

9. In view of the above finding, the present application, with or without claim 9, does not meet the requirements of the EPC and the appeal has to be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

D. Sauter W.J.L. Wheeler