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D E C I S I O N
of 7 May 2003

Case Number: T 0971/00 - 3.4.3

Application Number: 92106728.6

Publication Number: 0510557

IPC: H01L 29/73

Language of the proceedings: EN

Title of invention:
Resonant tunneling transistor

Applicant:
NIPPON TELEGRAPH AND TELEPHONE CORPORATION

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no) - objection technical problem"

Decisions cited:
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Catchword:
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Case Number: T 0971/00 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 7 May 2003

Appellant: NIPPON TELEGRAPH AND TELEPHONE CORPORATION
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Representative: Hoffmann, Klaus-Dieter, Dipl.-Ing.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 27 April 2000 refusing European patent application No. 92 106 728.6 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: V. L. P. Frank
J. P. B. Seitz

Summary of Facts and Submissions

I. The appeal lies from the decision of the Examining Division dated 27 April 2000 refusing European patent application No. 92 106 728.6 on the ground that the subject-matter of claim 1 was not new having regard to the prior art document

D1: Patent Abstracts of Japan, Vol. 11, No. 351 (E-557), 17 November 1987 & JP-A-62 128 562.

Reference was also made in the examination proceedings to the following prior art document:

D2: Proceedings IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, 7-9 August 1989, pp. 255-264

II. The appellant (applicant) lodged an appeal on 26 June 2000, paying the appeal fee the same day. The statement setting out the grounds of appeal was filed on 27 July 2000. Oral proceedings were requested as an auxiliary measure.

The appellant requested the reversal of the decision under appeal and the grant of a patent on the basis of amended claims 1 to 8 submitted together with the statement of grounds of appeal.

III. With the Fax dated 5 May 2000 the appellant's representative informed the Board that the appellant had decided not to attend the oral proceedings scheduled to take place on 7 May 2000.

As announced, the appellant was not represented at the oral proceedings which were held by the Board as scheduled.

IV. The wording of the independent claim is as follows:

"1. A resonant tunnelling transistor comprising:
a first semiconductor layer (22) having an n-type conductivity and serving as a collector layer;
a second semiconductor layer (24) having a p-type conductivity and serving as a base layer and forming a quantum well;
a third semiconductor layer (26) having the n-type conductivity, serving as an emitter layer;
a fourth semiconductor layer (23) serving as a first tunnelling barrier layer against either of electrons and holes in said first and second seminconductor *(sic)* layers (22; 24); and
a fifth semiconductor layer (25) serving as a second tunnelling barrier layer against either of electrons and holes in said second and third semiconductor layers (24; 26);
wherein
said first (22), second (24), third (26); fourth (23) and fifth (25) semiconductor layers are sequentially stacked in an order of said first, fourth, second, fifth, and third semiconductor layers,
characterized by the combination of the features that said second semiconductor layer (24) includes at least one further semiconductor layer (41; 41a; 41b), each further semiconductor layer (4; 41a; 41b) *(sic)* serving as a further tunnelling barrier against either of electrons and holes, and dividing said second semiconductor layer (24) into second semiconductor layer portions (24a, 24b, 24c, 125, 127) adjoining said

each further semiconductor layer (41; 41a; 41b), each of said second semiconductor layer portions (24a, 24b, 24c, 125, 127) forming a quantum well,
that the second (24), fourth (23), and fifth (25) semiconductor layers form a resonant tunnelling structure; and
that each of said semiconductor layer portions (24a, 24b, 24c, 125, 127) of said semiconductor layer (24) has an impurity concentration which is gradually decreased from a central portion to a peripheral portion in a direction of thickness."

V. The arguments of the appellant can be summarized as follows:

The state of the art described in the application in suit is closer to the invention than the disclosure of document D1. This document does not disclose a resonant tunnelling structure, since the figures do not show emitter-base voltage-current characteristics having a large P/V ratio (the so called peak-to-valley ratio) similar to that shown in Fig. 10 of the application. Moreover, the base region in the resonant tunnelling transistor (RTT) according to the present invention is not formed by a super-lattice structure as disclosed in document D1. Furthermore, document D1 does not give any indication in relation to the impurity concentration distribution within the layer portions forming the base region. Document D2 discloses only the general technological background of the present invention and does not give any indication for increasing the P/V ratio of a RTT. The impurity concentration profile in the base region according to claim 1 is not merely a

matter of normal design procedure, but leads to the outstanding effect of the present invention. It is, furthermore, not possible to combine the teaching of documents D1 and D2 without an inventive step.

The applicant further submitted that the following evidence supports the inventiveness of the claimed invention: the invention is economically successful, it overcomes difficulties (reduced negative transconductance, distortion of output waveform), it satisfies a long-standing demand, it has improved performance and enhanced efficiency, and it has a reduced cost of production.

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments*

The amended independent claim 1 is a combination of claims 1 and 9 as originally filed. It is, moreover, not expedient to analyse in detail the amendments made to the claims, as the appellant's request fails for the reasons which follow.

3. *Novelty (Article 54 EPC)*

3.1 Document D1 discloses a semiconductor device comprising a n-type collector region 3, a p-type base region 2, 2' and a n-type emitter region 1. The base region is formed of a supperlattice structure formed of alternating layers of AlGaAs and GaAs. The AlGaAs layers 2' have a larger bandgap than the GaAs layers 2

and form, therefore, tunnelling barriers between the GaAs layers and between these layers and the collector and emitter regions. The period and the barrier height of the supperlattice forms mini-bands in the base region so that only electrons with energies falling within the permissible bands can pass the base and reach the collector (cf. Figs. 1 and 2, Abstract). The base-emitter voltage-current characteristic displays, therefore, current peaks E1 and E2 when the successive permissible energy bands are traversed (cf. Fig. 3). The semiconductor device, therefore, has a negative transconductance under base voltage bias condition.

The characteristic current-voltage curve shown in Fig. 3 of document D1 is similar to the curve displayed in Fig. 10 of the application in suit, in particular, as both figures are merely schematic and do not allow any quantitative comparison, since they do not include numerical values or scales.

For these reasons, in the Board's view, the semiconductor device disclosed in document D1 is a resonant tunnelling transistor (RTT) in the sense of the invention as claimed.

3.2 The Board concurs, however, with the appellant that document D1 does not disclose the impurity concentration profile within the GaAs layers 2 forming the base region as claimed. In particular, it is not disclosed in document D1 that the impurity concentration in these layers decreases gradually from the central to the peripheral portion in the direction of their thickness (ie the last feature of claim 1).

Consequently, the subject-matter of claim 1 is new.

4. *Inventive step (Article 56 EPC)*

4.1 The appellant has contended that the state of the art discussed in the application in relation to Figs. 1 to 6 is closer to the present invention than the disclosure of document D1.

According to the application in suit, the principal object of the invention is to increase the current gain and negative transconductance of the transistor, to reduce the distortion of a transmitted waveform and to improve the high frequency transistor's characteristics (cf. column 5, lines 10 to 29 of the published application). These effects are achieved by dividing the base region into a plurality of semiconductor layer portions (cf. ibid, column 5, lines 30 to 51).

The essential concept underlying the invention is, therefore, the replacement of the single layer base region of the RTTs of the state of the art by a multilayered base region.

However, in all the prior art transistors disclosed in the application the base region is formed by a single layer of semiconductor material. In contrast thereto, the base layer of the transistor disclosed in document D1 comprises several layers of semiconductor material separated by tunnelling barrier layers. This structure is, therefore, the state of the art which is closer to the invention than the state of the art described in the application in suit.

4.2 The RTT according to claim 1, therefore, differs from the semiconductor structure disclosed in document D1 only in that the impurity concentration profile of the

layers forming the base region gradually decreases from the central to the peripheral portion in the thickness direction.

4.3 In assessing inventive step, the Boards of Appeal generally apply the "problem and solution approach". This approach consists in (a) identifying the closest state of the art, (b) assessing the technical effects achieved by the claimed invention when compared with the closest state of the art, (c) defining the technical problem addressed by the invention in view of the technical effects (this is often termed as the "objective technical problem") and (d) examining if the skilled person would regard as obvious the claimed technical features for solving the objective technical problem, having regard to the state of the art in the sense of Article 54 (2) EPC.

4.4 It is, therefore, necessary to determine the technical effects achieved by the feature differentiating the transistor according to claim 1 from the transistor disclosed in document D1, ie the impurity concentration profile of the layers forming the base region.

In this connection the application in suit does not disclose any technical effects which can be attributed to the doping profile of the base region. Prior art document D2 discloses a bipolar quantum well resonant tunnelling transistor in which a p-type base region is formed by a single layer of semiconductor material. The emitter and collector regions are separated from the base region by tunnelling barriers. In the formation of the p-type base region having an overall thickness of 15 nm, only a 5 nm thick central portion is doped p-type (cf. page 259, last paragraph).

Although not disclosed in document D2, it is evident that the p-type dopant diffuses out from the central portion of the base region into the adjacent undoped regions and creates a gradually decreasing impurity concentration profile in the base region as specified by the last feature of claim 1.

A skilled person in the art, in the Board's view, would deduce that a homogeneous doping of the base region may lead to contamination of the adjacent tunnelling barriers by the dopant atoms due to their outward diffusion from the doped region. Consequently, the person skilled in the art understands from document D2 that surrounding the doped, central portion of the quantum well by undoped regions avoids the contamination of the tunnelling barriers.

4.5 For these reasons, in the Board's view, the objective technical problem solved by the present invention is to avoid the contamination of the tunnelling layers by the p-type dopant of the base layer.

4.6 Accordingly, a skilled person would dope only the center portions of the multiple layers forming the base region of the semiconductor device disclosed in document D1 so that the tunnelling layers are not contaminated by the doping atoms of the base layer. The subject-matter of claim 1 was thus obvious having regard to prior art documents D1 and D2.

4.7 The appellant has contended that the outstanding features of the transistor according to claim 1, ie the increase in current gain and negative transconductance, and reduced waveform distortion, are due to the specific doping profile employed in the base region.

This argument, however, is not convincing, since the application in suit does not disclose any technical effect which is specifically related to the doping of the base layers (cf. column 7, lines 25 to 39 of the published application). The increase in current gain and negative transconductance, and the reduced distortion of the transmitted waveform are achieved, according to the application, by the use of a multilayer base region and not by the impurity doping profile (cf. ibid, column 5, lines 10 to 51). The use of a multilayer base region, as discussed above, is however known from document D1.

4.8 The appellant has also argued that the fact that the invention is economically successful, overcomes difficulties in the state of the art, satisfies a long-standing demand, has improved performance and enhanced efficiency, and has a reduced cost of production should be seen as a proof of inventiveness.

No evidence in support of these alleged facts has, however, been submitted by the appellant. Moreover, even if this evidence would have been available to the Board, it is the established case law of the Boards of Appeal that these secondary indicia in determining inventive step are no substitute for the technically skilled assessment of the invention vis-à-vis the state of the art (cf. Case Law of the Boards of Appeal, 4th edition 2001, I.D.7).

4.9 For the foregoing reasons, it is the Board's judgement that the subject-matter of claim 1 does not involve an inventive step in the sense of Article 56 EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

P. Martorana R. K. Shukla