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D E C I S I O N
of 2 April 2003

Case Number: T 0904/00 - 3.5.1

Application Number: 95400552.6

Publication Number: 0674411

IPC: H04L 12/56, H04Q 11/04

Language of the proceedings: EN

Title of invention:
Virtual interconnection memory especially for communication between terminals operating at different speeds

Applicant:
TEXAS INSTRUMENTS FRANCE, et al

Opponent:
-

Headword:
Interconnection-point memory/TEXAS INSTRUMENTS

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0904/00 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 2 April 2003

Appellants: TEXAS INSTRUMENTS FRANCE
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 3 March 2000 refusing European patent application No. 95 400 552.6 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: S. V. Steinbrener
Members: A. S. Clelland
E. Lachacinski

Summary of Facts and Submissions

I. European patent application No. 95 400 552.6 was refused by a decision of the examining division dated 3 March 2000 on the ground that the subject-matter of claim 1 lacked an inventive step. The following document was cited:

D1: EP-A-0 504 710.

II. The applicants appealed, requesting that the decision be set aside and that the application be allowed to proceed on the basis of claims of a newly filed main request, corresponding in substance to the originally filed claims. It was also requested that the application be referred back to the examining division if the Board considered it to be acceptable apart from formal deficiencies. A conditional request was made for oral proceedings. The appellants also filed claims of first and second auxiliary requests and indicated the scope of claims of intended third and fourth auxiliary requests, but did not file them.

III. In an Annex to a summons to oral proceedings the Board raised issues of clarity under Article 84 EPC in respect of claims of the main and first auxiliary requests. The Board also raised the question of novelty and inventive step with respect to the claims of various of the newly filed requests and referred to the document cited by the examining division and, *inter alia*, to the following document:

D3: IEICE Transactions on Electronics, vol. E76-C, July 1993, No. 7, Tokyo, Pages 1094-1100, Kondoh et al: "A Shared Multibuffer Architecture for

High-Speed ATM Switch LSIs".

D3 was cited in the European Search Report and introduced into the proceedings by the Board, making use of its powers under Article 114(1) EPC.

IV. In a response to the Board's comments the appellants argued that the claims of all requests were novel and inventive. Claims of a fifth auxiliary request were filed.

At the oral proceedings held on 2 April 2003, the appellants withdrew all the existing requests and filed a new sole request based on the claims of the fifth auxiliary request. It was requested that the decision under appeal be set aside and a patent granted on the basis of claims 1 to 8 of this request.

V. Claim 1 reads as follows:

"Interconnection-point memory including an array of N1 data input buses (DATA-IN) intended to be connected to a first plurality of N1 data-sender devices, an array of N2 data output buses (DATA-OUT) intended to be connected to a second plurality of N2 data-receiver devices, and interconnection means for connecting the said array of data input buses to the said array of data output buses, wherein the said interconnection means include a third plurality of N3 switching memories (17),

wherein each switching memory (17) is provided with:

- a data input (Din),
- a write address input (W-addr),
- a data output (Dout),

- a read address input (R-addr),

characterized in that

each switching memory (17) is a first in - first out device,

the interconnection point memory further comprises:

- N1 input address buses (Addr-in) associated in N1 input buses (Rj) to the data input buses (DATA-IN),

- N2 output address buses (Addr-out)associated in N2 output buses (Ck) to the N2 output data buses (DATA-OUT),

the data input (Din) of said specified switching memory (17) is connected to all of the plurality of N1 data input buses (DATA-IN) by data input multiplexer circuits (24a), able to connect any one of the plurality of N1 data input buses (DATA-IN) to said data input (Din) of said specified switching memory (17),

the data output (Dout) of said specified switching memory (17) is connected to all of the plurality of N2 data output buses (DATA-OUT) by data output multiplexer circuits (24a'), able to connect any one of the plurality of N2 data output buses (DATA-OUT) to said data output (Dout) of said specified switching memory (17),

the write address input (W-addr) of said specified switching memory (17) is connected to all of the plurality of N1 input address buses (Addr-In) by address input multiplexer circuits (24b), able to connect any one of the plurality of N1 input address buses (Addr-in) to said write address input (W-addr) of said specified switching memory (17),

the read address input (R-addr) of said specified switching memory (17) is connected to all of the plurality of N2 output address buses (Addr-out) by

address output multiplexer circuits (24b'), able to connect any one of the plurality of N2 output address buses (Addr-out)to said read address input (R-addr) of said specified switching memory (17),

the data and address input multiplexer circuits (24a, 24b) multiplexing the write address input (W-addr) and the data input (Din) of said specified switching memory (17) are enabled or disabled by a same input control register (S [j, m]) associated to said specified switching memory (17), on the basis of the binary content of said input control register (S [j, m]),

the data and address output multiplexer circuits (24a', 24b') multiplexing the read address input (R-addr) and the data output (Dout) of said specified switching memory (17) are enabled or disabled by a same output control register (S [j, m]) associated to said specified switching memory (17), on the basis of the binary content of said input control register (S [j, m]),

so as to ensure interconnection between a specified input bus (Rj) and at least one specified output bus (Ck)."

Claims 2 to 8 are dependent on claim 1.

VI. At the end of the oral proceedings the Board announced its decision.

Reasons for the Decision

1. Admissibility of the appeal.

The appeal satisfies the requirements mentioned in

Rule 65(1) EPC and is consequently admissible.

2. *Amendments*

The Board is satisfied that the amendments made to claim 1 meet the requirement of Article 123(2) EPC (added subject-matter).

3. *Technical background to the invention*

3.1 In high-speed data communications, asynchronous transfer mode (ATM) networks can provide bearer services with a specified quality of service for differing traffic types (see e.g. D3, page 1094). ATM is connection-oriented, the cells being of a fixed 53-byte length and each containing an address to which the cell is being sent; all cells bearing the same address follow the same path, referred to as a virtual channel in ATM terminology. Various forms of service at differing speeds can be provided by an ATM network, depending on predetermined parameters such as peak cell rate, sustained cell rate and burst tolerance, together with the desired quality of service. A difficulty which arises in ATM networks is the need to switch individual cells to follow their predetermined virtual path, giving rise to the need for high-speed switches with a minimum delay within the switch. Such switches are designed to enable cells arriving on one of a plurality of input ports to be passed with a minimum of delay to a desired output port or ports, some form of buffering being required since the cells are asynchronous and the data rate at input and output is not necessarily the same; further reasons for buffering, not given in the application but discussed in the prior art, are the need to avoid cell contention when two cells might be

outputted by the same port simultaneously.

3.2 One form of switch which is used in ATM networks is the interconnection-point switch in which a switching matrix connects the input and output ports. The required buffer memories can be provided by locating a buffer memory at each crossover point of the matrix, see Figure 5 of the application, but this is expensive in terms of the number of transistors required and would need an excessive die area if constructed in integrated form. An alternative solution, shown in Figure 6 of the application, is to provide memories only at the input ports, but this does not solve the problem of cell blocking and results in a degradation of switch performance. The claimed invention seeks to overcome the deficiencies of prior art switches by providing a fixed number of buffer memories, less than the number of crossover points, which are connected at crossover points only as and when necessary and as a function of instantaneous communication needs between the input and output ports. As claimed, the buffer memory is a first in-first out (FIFO) device.

4. *Inventive step*

4.1 Although claim 1 includes a considerable amount of highly specific detail relating to the interconnection of input and output address and data buses, the Board understands from the presentation of the invention at the oral proceedings that the main difference seen over the prior art is the ability to connect a specified switching memory to any desired data input and data output bus. In the course of the oral proceedings it became clear that this is known from document D3.

4.2 D3, published before the priority date of the application, discloses an ATM switch in which, referring to page 1094, right-hand column, multiple buffer memories are provided which can be "accessed in parallel via crosspoint switches located immediately before and after the buffer memories". This is said to have the advantages that the cycle time of the buffer memory is reduced, so that high speed operation is possible, and that an integrated switch does not need a large die area. The basic design is shown in Figure 1 on page 1095 and can be seen to comprise two crosspoint switches, respectively connected to the input and output ports, and connected to each other by a plurality of buffer memories of RAM type which are stated at page 1095, left-hand column, to be "shared among all input and output ports and crosspoint switches". The Board accordingly understands that the basic switch architecture which is the subject of the application is known from D3.

4.3 Although it was argued by the representative in the course of the oral proceedings that D3 does not disclose buffer memories of the FIFO type, the Board notes that page 1095, right-hand column refers to the storage of address information for a cell in an address queue, implying that in normal operation the cells are read in and out sequentially. This operation is shown in Figures 2 and 3 on page 1095; although the Board accepts that the RAM memory used enables a so-called "multiple-read operation" in order to ameliorate the problem of blocking, nevertheless the data is generally read in and read out sequentially in accordance with the first-in, first-out principle.

4.4 Turning now to the specific details claimed in claim 1,

D3 (see Figure 1) discloses an interconnection-point memory including an array of N1 data input buses intended to be connected to a first plurality of N1 data-sender devices, an array of N2 data output buses intended to be connected to a second plurality of N2 data-receiver devices, and interconnection means for connecting the array of data input buses to the array of data output buses, wherein the interconnection means include a third plurality of N3 switching memories. Referring to Figures 6 and 7 of D3 at page 1097, it can be seen that each switching memory is provided with a data input, a write address input, a data output and a read address input. As discussed above the individual switching memories are RAMs configured to operate as first-in, first-out devices. D3 states at page 1095, left-hand column, that the memories are "shared among all input and output ports and crosspoint switches", implying that each switching memory is able to connect to any one of the plurality of data input buses and data output buses. The remainder of the claim is concerned with the manner in which the individual switching memories are addressed; input and output address buses are specified in addition to the input and output data buses, the write and read address inputs of each memory being connected to respective buses by multiplexer circuits able to connect a bus to a specified write or read address input. The Board notes that it is common general knowledge in the art to separate data and address buses and to use a single address bus; this can be seen from Figures 6 and 7 of page 1097 of D3, where addressing is provided by a CONTROL block which has a 7-bit address bus.

4.5 The subject-matter of claim 1 accordingly differs from the disclosure of D3 in that the claim requires

separate input and output address buses and input and output control registers which enable or disable data and address input and output multiplexer circuits. The Board observes that the reference to "multiplexer" circuits is apparently erroneous, all other references to multiplexers having been deleted from the claim. What is meant by "multiplexer" circuits is apparently the provision of switches in order to enable specific memories in dependence on a chosen address, see point 4.9 below. This would appear to be a self-evident requirement of any addressing arrangement. In D3 moreover a single control block controls both the crosspoint switches and the memory addressing, implying that common input and output control registers are provided.

4.6 The provision of separate input and output address buses would appear to be a matter of normal practice in the memory art, well-known to the skilled person and not involving the exercise of invention.

4.7 The subject-matter of claim 1 of the sole request accordingly lacks an inventive step having regard to the disclosure of D3.

4.8 The representative argued that D3 was not relevant to the claimed invention because it failed to appreciate that memories could be shared between a number of input and output buses. In D3 the number of memories was dependent on the number of input ports whereas in accordance with the application only the degree of blockage which was acceptable determined the number of memories. The Board notes however that claim 1 is not limited to any specific number of memories, or any specific manner of choosing the number of memories, but

merely refers to "a third plurality of N3 switching memories". The claim does not exclude the case of N1=N3, where N1 is the number of data input buses.

4.9 Although in the response to the communication accompanying the summons to oral proceedings the representative argued that D3 differed from the claimed invention in not providing multiplexers, it became clear in the course of the oral proceedings that the expression "multiplexer" was not used in the normal sense of the expression. It appears rather that what is referred to as a "multiplexer" is in fact a switch which has the function of connecting the data and address buses to respective memory data and address inputs, or alternatively outputs. This can be best seen in Figure 13 of the application. The Board infers from this figure and the associated description that the "multiplexers" are in fact components of the crosspoint switches and perform, as discussed above, a switching function in order to connect a specific input by way of a memory to a specific output. Although D3 does not discuss the construction of the crosspoint switches it uses, it appears to the Board that the so-called "multiplexers" are merely a standard manner in which switching can be performed.

5. Since claim 1 is not allowable it follows that the request as a whole is not allowable and the appeal must be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Kiehl S. V. Steinbrener