BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [X] To Chairmen
(D) [ ] No distribution

D E C I S I O N
of 20 August 2003

Case Number: T 0758/00 - 3.4.3

Application Number: 90113691.1

Publication Number: 0409174

IPC: H01L 27/148

Language of the proceedings: EN

Title of invention:
Structure of solid-state image sensing devices

Applicant:
SONY CORPORATION

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 123(2), 56

Keyword:
"Admissibility of the amendments (yes)"
"Inventive step (yes, after amendments)"

Decisions cited:
-

Catchword:
-

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0758/00 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 20 August 2003

Appellant: SONY CORPORATION
7-35, Kitashinagawa 6-chome
Shinagawa-ku
Tokyo (JP)

Representative: Schmidt-Evers, Jürgen, Dipl.-Ing.
Patentanwälte
Mitscherlich & Partner
Postfach 33 06 09
D-80066 München (DE)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 29 February 2000 refusing European application No. 90113691.1 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: M. Chomentowski
J. van Moer

Summary of Facts and Submissions

I. The European patent application No. 90 113 691.1 (Publication No. 0 409 174) was refused by the examining division on 29 February 2000 on the grounds that its subject-matter according to the main and auxiliary requests lacked an inventive step.

II. Claim 1 of the *main request* forming the basis of the decision of the examining division reads as follows:

"1. A solid-state frame interline type (FIT) imager comprising:

(a) an image portion (21) comprising a plurality of photo receiving elements arranged in a matrix form and a plurality of first vertical registers having first transfer electrodes (IM) for transferring in the vertical direction signal charges read out from the plurality of photo receiving elements;

(b) a storage portion (22) comprising a plurality of second vertical registers having second transfer electrodes (ST) for temporarily storing the signal charges transferred from the image portion;

(c) **a plurality of horizontal registers**, each having third transfer electrodes for transferring the signal charges from said storage portion in the horizontal direction;

(d) first shunt wirings (29) formed independently on the first transfer electrodes (IM) and connected to said first transfer electrodes (IM) said first shunt

wirings being used for applying first drive pulses (IV) from a first bus line to the first transfer electrodes; and

(e) second shunt wirings (30) provided separately from said first shunt wirings and formed independently on the second transfer electrodes and connected to said second transfer electrodes (ST), said second shunt wirings being used for applying second drive pulses (SV) from a second bus line independent from the first bus line to the second transfer electrodes, said imager further comprising:

a control gate (3) for controlling the transfer of signal charges between said horizontal registers in synchronization with said second drive pulses."

The expression "a plurality of horizontal registers" at the beginning of feature (c), has been highlighted by the Board as an amendment which, in accordance with the decision under appeal (cf. paragraph 2.1 of the reasons), was made at the request of the applicant during the oral proceedings before the examining division for replacing the expression "at least one horizontal register", which amendment is not shown in the copy of the claim annexed to the decision.

III. The reasoning in the decision of the examining division relevant to the present appeal can be summarized as follows:

Main request

Document

D3: Patent Abstracts of Japan, vol. 12, no. 369 (E-665) 3216 & JP-A-63-120463

is the closest prior art document and shows in Figure 5 a solid state frame interline type (FIT) imager comprising the following features:

(a') an image portion (A) comprising a plurality of photo receiving elements (7) arranged in a matrix form and a plurality of first vertical registers (9) having first transfer electrodes for transferring in the vertical direction signal charges read out from the plurality of photo receiving elements;

(b') a storage portion (B) comprising a plurality of second vertical registers having second transfer electrodes for temporarily storing the signal charges transferred from the image portion;

(c') an horizontal register (c) having third transfer electrodes;

(d') first wirings formed independently and connected to the first transfer electrodes and connected to said first transfer electrodes said first wirings being used

for applying first drive pulses ($_{V1}$ to $_{V4}$) from a first bus line to the first transfer electrodes; and

(e') second wirings provided separately from said first shunt wirings and formed independently and connected to said second transfer electrodes, said second shunt wirings being used for applying second drive pulses ($_{M1}$ to $_{M4}$) from a second bus line independent from the first bus line to the second transfer electrodes.

However, contrary to the claimed FIT imager, in the known device there is neither a plurality of horizontal registers with a control gate for controlling transfer of charge between the horizontal registers, nor are the first and second shunt wirings.

As regards the feature of a plurality of horizontal registers and a corresponding controlling gate, the application in suit mentions at page 2, lines 4 to 14 that "Japanese Patent Application Second Publication (Examined) No. Heisei 1-13676 published on March 7, 1989" discloses an imager in which a plurality of horizontal registers are arranged in parallel and signal charges generated by photo receiving elements are distributed in this plurality of horizontal registers so that an improvement in integration of pixels in the horizontal direction can be achieved. Reference can also be made to document

D1: EP-A-0 127 223

mentioning that a plurality of horizontal registers allow to obtain a maximum resolution in the horizontal direction. Accordingly, a skilled person will select

the provision of a plurality of horizontal registers (which provision implies control gates for charge transfer between these horizontal registers) whenever a maximum resolution in the horizontal direction is desired. Accordingly, item (c) and the two last lines of claim 1 are obvious.

Concerning the feature of a shunt wiring, the problem of distorted signals resulting from the R,C components of an electrode is already dealt with in Figure 8 of document D3, showing the R,C components of an electrode, which is similar to Figure 3B of the original application, and further showing distortion of a square pulse due to these RC components. The solution to this problem of distorted signals is to reduce electrode resistance by providing a laminate of polysilicon and silicide (see the English abstract ("Purpose")).

The problem of signal distortion due to R,C components of an electrode is also dealt with in document

D4: DE-A-3 436 632,

where Figure 1B is similar to Figure 3B of the original application and Figure 2 shows that a square signal is distorted into a sine wave.

The solution provided by document D4 is a shunt wiring with an aluminium wiring shorting portions of a polysilicon wiring. If a skilled person is faced with the problem of signals distorted by R,C components on an electrode, simple routine experiments will show whether the shunt wiring of document D4 is better than

the laminated wiring of document D3. Since aluminium used in document D4 is known to have a lower resistivity than silicide used in document D3, the skilled person would expect that the shunt wiring of document D3 is better.

Although the English abstract of document D3 is silent on bus wiring, the document (cf. Figure 8) addresses the same problem as the present application (cf. Figure 3B). Even if document D3 would solve the problem of a distorted signal by means of a transfer electrode having a laminate structure of polysilicon and silicide, it would still be obvious to solve the problem of a distorted signal by shunt wiring for the bus wiring because this solution is known from document D4 also concerning distorted signals and providing an alternative solution. There is even an incentive to apply the solution of document D4 to the FIT imager of document D3 in view of the lower resistivity of aluminium used in document D4 for shunt wiring with respect to the higher resistivity of the silicide used for the laminate wiring in document D3.

Therefore, the subject-matter of claim 1 of the main request lacks an inventive step.

IV. The applicant lodged an appeal against this decision on 11 April 2000 paying the appeal fee on the same day. A statement setting out the grounds of the appeal was received on 29 June 2000.

V. In response to communications and telephonic consultations with the Board, the appellant filed with the letters dated 22 July 2003 and 5 August 2003 new

patent application documents and requested that the decision under appeal be set aside and a patent be granted with the following application documents:

Description: Pages 1 to 11 filed with letter dated 22 July 2003;

Claims: Nos. 1 to 10 filed with letter dated 5 August 2003;

Drawings: Sheets 1/3 and 2/3 as filed;
Sheet 3/3 filed with letter dated 28 June 1999.

Claim 1 reads as follows:

"1. A solid-state frame interline type (FIT) imager comprising:

(a) an image portion (21) comprising a plurality of photo receiving elements arranged in a matrix form and a plurality of first vertical registers having first transfer electrodes (IM) for transferring in the vertical direction signal charges read out from the plurality of photo receiving elements;

(b) a storage portion (22) comprising a plurality of second vertical registers having second transfer electrodes (ST) for temporarily storing the signal charges transferred from the image portion (21);

(c) a plurality of horizontal registers, each having third transfer electrodes for transferring the signal charges from said storage portion (22) in the

horizontal direction **sharing the signal charges with respective ones thereof**;

(d) first shunt wirings (29) **provided over** the first transfer electrodes (IM) and connected **at selected locations** to said first transfer electrodes (IM) said first shunt wirings (29) being used for applying first drive pulses (IV) from a first bus line to the first transfer electrodes (IM); and

(e) second shunt wirings (30) provided separately from said first shunt wirings (29) and **provided over** the second transfer electrodes (ST) and connected to said second transfer electrodes (ST) **at selected locations**, said second shunt wirings (30) being used for applying second drive pulses (SV) from a second bus line independent from the first bus line to the second transfer electrodes (ST), said imager further comprising:

a control gate (3, 14) for controlling the transfer of signal charges between said horizontal registers in synchronization with said second drive pulses (SV)."

The main amendments with respect to the main request forming the basis of the appealed decision have been highlighted by the Board:

"**provided over**" in features (c) and (d) replace "formed independently on";

"**sharing the signal charges with respective ones thereof**" has been added at the end of feature (c) and

"**at selected locations**" has been inserted in features (d) and (e).

Claims 2 to 10 are dependent claims.

VI. The appellant submitted substantially the following arguments in support of his request:

In the consideration of inventive step it is not allowed to interpret prior art documents with the knowledge of the solution proposed in the application. The prior art documents should be interpreted on the basis of the problem posed in the closest prior art document.

The teaching of document D3 is rather speculative and, even when starting therefrom, document D4 is not of any relevance to the claimed invention.

Furthermore, due to the speculative character of the teaching of document D3, even if document D4 were to be taken into account, the person skilled in the art would not deduce from both said documents the teaching of claim 1.

Reasons for the Decision

1. The appeal is admissible.

2. *Formal requirements*

As compared to claim 1 of the main request forming the basis of the contested decision, claim 1 now specifies in feature (c) that the plurality of horizontal registers of the imager has transfer electrodes for transferring the signal charges from the storage portion in the horizontal direction, **sharing the signal charges with respective ones thereof.** This feature is based on the only two independent claims of the application as filed, i.e., claims 1 and 11, which specified with respect to feature (c) that the plurality of horizontal registers has transfer electrodes for transferring the signal charges from the storage portion in the horizontal direction, **sharing the signal charges with respective ones thereof**. The same feature was repeated in the description of the application as filed (see page 4, line 33 to page 5, line 1 and page 5, lines 14 to 18; see also page 2, lines 4 to 14) with respect to the invention as well as to a corresponding acknowledged device.

This is consistent with the corresponding parts of the description wherein this feature is derivable as an important feature of the invention.

The further amendments in features (d) and (e) of claim 1 consist in the substitution of the expressions "... shunt wirings **provided over** the .... transfer electrodes and connected **at selected locations** to said

... transfer electrodes" for the corresponding expressions "... shunt wirings formed independently on the ... transfer electrodes (IM) and connected to said ... transfer electrodes", which is based on the application as filed and which clearly specifies the structure of shunt wirings, e.g. as shown in Figure 3.

In this respect, it is to be noted that dependent claim 2 and the claims 3 to 10 depending therefrom comprise features of shunt wirings of claim 1 and of their use for reducing the specific resistance along the respective drive pulse transmission path and of further parts of the imager, based on the first and second embodiment which were disclosed originally. Indeed, it is to be noted that claim 1 is the only preferred embodiment remaining in the description and corresponds to Figure 6. The dependent claims recite features which are taken from those originally mentioned first and second preferred embodiments, whereby said features in the description remain as "additional developments to be used with a solid state frame interline type imager according to the present invention".

In the Board's judgement, these amendments are admissible since it was stated in the application as filed (see page 10, lines 23 to 26) that a combination of the first or second preferred embodiment with the third preferred embodiment can be applied to the solid-state image sensing device according to the present invention.

The further amendments result in the claims being consistent with the description and drawings, in agreement with the application as filed.

Therefore, the application satisfies the requirement of Article 123(2) EPC that a European patent application may not be amended in such a way that it comprises subject-matter which extends beyond the content of the application as filed.

Moreover, the Board is satisfied that the claims comply with the requirement of clarity of Article 84 EPC.

3. *Inventive step*

3.1 Inventive step is the only remaining issue.

It has not been disputed that Figure 5 of JP-A-63-120463, i.e., the Japanese patent application corresponding to the patent abstract of document D3, shows a solid-state frame interline type (FIT) imager which is of the same type as the claimed device and can be considered as representing the closest prior art.

It has not been disputed either that this known device comprises only one horizontal register, and does not comprise a plurality of horizontal registers as in the claimed invention. Accordingly,

it does not comprise a control gate for controlling transfer of charges between the horizontal registers, and, moreover,

it does not comprise the feature that the control gate is for controlling the transfer of signal charges between these horizontal registers in synchronization with specific second drive pulses, i.e. with a circuitry for this purpose of the type shown in Figure 6 of the application.

The known device also does not comprise any first and second shunt wirings as recited in the present claim, and this has not been disputed either.

3.2 According to the application (see page 4, lines 18 to 29), it is an object of the invention to provide a structure of a solid-state image sensing device in which at least one of drive pulse transmission paths of a control gate for controlling transfer of signal charges transferred from vertical registers to horizontal registers in synchronization with first drive pulses and of transfer electrodes provided for driving vertical registers to transfer signal charges generated in a plurality of photo receiving elements can achieve reduced drive pulse signal propagation delays and reduced signal distortions.

3.3 Indeed, as regards the feature of a plurality of horizontal registers, a corresponding controlling gate and the improvements provided thereby, reference can be made to the document mentioned in the application as filed (see page 2, lines 4 to 14), and also to document D1.

Similarly, as regards the purpose of reducing the resistance of an electrode to increase the high-speed transfer frequency of a vertical transfer stage, to

improve the reduction effect of vertical smears and to improve a vertical transfer efficiency by a method wherein a transfer electrode constituting a vertical transfer part and a memory part is formed of laminated polysilicon and silicide, reference can be made to document D3 (see the "Purpose" of the patent abstract in English), or also to document D4 (see Figure 1B) dealing with the problem of distorted signals resulting from the R,C components of an electrode and solving this problem by providing a shunt wiring with an aluminium wiring shorting portions of a polysilicon wiring.

However, with respect to the question, whether it would be obvious to a skilled person to select the provision of a plurality of horizontal registers (which provision implies control gates for charge transfer between these horizontal registers) whenever a maximum resolution in the horizontal direction is desired, and to provide a shunt wiring with an aluminium wiring shorting portions of a polysilicon wiring, the following is to be noted:

Document D3 does not refer to a plurality of horizontal registers and to means associated to such a structure. It is thus only with the knowledge of the solution proposed by the invention, i.e., by hindsight, that the document can be interpreted to contain some of the features.

It has not been disputed that document D1, which discloses a frame transfer type imager, as well as the further prior art documents such as D4, concern imagers which are not directly related to a solid-state frame interline type (FIT) imager according to document D3 in

that they have a different structure and a different mode of operation.

Concerning the "Japanese Patent Application Second Publication (Examined) No. Heisei 1-13676 published on March 7, 1989" mentioned in the application at page 2, lines 4 to 14 as disclosing an imager in which a plurality of horizontal registers are arranged in parallel and signal charges generated by photo receiving elements are distributed in this plurality of horizontal registers so that an improvement in integration of pixels in the horizontal direction, there is no indication either as the to the type of imager referred to in the document.

Therefore, as convincingly argued by the appellant, taking into account the problem in the closest prior art document, i.e. document D3, it is only by hindsight, that is, by taking into account the solution proposed by the application in suit, that a combination with the reported teaching of the cited Japanese document "No. Heisei 1-13676" or with that of document D1, relevant for not clearly defined imagers or for other types of imagers, can be considered as obvious, and this is not allowable for assessing inventive step.

Consequently, in view of the findings in the preceding paragraph, it is not considered necessary to assess, whether a shunt wiring structure comprising aluminium shorting portions on a polysilicon electrode layer as disclosed in document D4 for an imager of an unspecified type would be an obvious alternative for

the electrode structure of the FIT imager of document D3.

Therefore, in the Board's judgement, the subject-matter of claim 1 involves an inventive step in the sense of Article 56 EPC.

Consequently, claim 1 is patentable in the sense of Article 52(1) EPC. Claims 2 to 10 concern particular embodiments and are patentable

Therefore, a patent can be granted on this basis (Article 97(2) EPC).

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the examining division with the order to grant a patent on the basis of the following application documents:

Description: Pages 1 to 11 filed with letter dated 22 July 2003;

Claims: Nos. 1 to 10 filed with letter dated 5 August 2003;

Drawings: Sheets 1/3 and 2/3 as filed;
Sheet 3/3 filed with letter dated 28 June 1999.

The Registrar: The Chairman:

U. Bultmann R. K. Shukla