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D E C I S I O N
of 11 July 2002

Case Number: T 0615/00 - 3.5.2

Application Number: 95113545.8

Publication Number: 0686976

IPC: G11C 16/06

Language of the proceedings: EN

Title of invention:

Data management system for programming-limited type
semiconductor memory and IC memory card having the data
management system

Applicant:

FUJITSU LIMITED

Opponent:

-

Headword:

-

Relevant legal provisions:

EPC Art. 76(1), 123(2)

Keyword:

"Divisional application extending beyond the content of the
earlier application (after amendment - no)"

Decisions cited:

-

Catchword:

-



Case Number: T 0615/00 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 11 July 2002

Appellant: Fujitsu Limited
1015, Kamikodanaka
Nakahara-ku
Kawasaki-shi
Kanagawa 211 (JP)

Representative: Seeger, Wolfgang, Dipl.-Phys.
Georg-Hager-Strasse 40
D-81369 München (DE)

Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 27 January 2000
refusing European patent application
No. 95 113 545.8 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: M. Ruggiu
B. J. Schachenmann

Summary of Facts and Submissions

- I. The applicant appealed the decision of the examination division refusing European patent application No. 95 113 545.8, which is a European divisional application of earlier European patent application No. 92 120 081.2.

The reason for the refusal was essentially that the subject-matter of the present application extended beyond the content of the earlier application as filed, in particular because some features of claim 1 of the earlier application as filed were not contained in the independent claim of the present application.

- II. Claim 1 of the earlier application as originally filed was as follows:

"A data management system for a programming-limited type semiconductor memory (M) which is programmable a limited number of times and which includes a plurality of storage areas, characterized in that the data management system comprises:

management means (1) for managing, for each of the storage areas, the number of times that programming has been performed; and

control means (2), coupled to said management means for selecting one of the storage areas for which programming has been performed the smallest number of times and for having input data written into a selected one of the storage areas, so that all the storage areas can be equally programmed."

III. Independent claim 10 of the present application as originally filed was as follows:

"A flash memory control apparatus characterized in that there are provided:

a flash memory (2) having a memory region which is divided into a plurality of sectors each including a logical address part (10) for storing a logical address of the sector, an attribute management field or erasure managing part (11) for storing information which indicates at least whether or not the sector may be erased, and a data part (12) for storing data; and

control means (1), coupled to said flash memory (2), for making access to an arbitrary sector of said flash memory (2) by specifying the logical address of the arbitrary sector."

The originally filed description and the figures of the present application are identical to the originally filed description and figures of the earlier application.

IV. In response to communications from the board, the appellant amended the claims and the description of the present application and requested the grant of a patent on the basis of the following documents:

description: pages 1, 2 filed with a fax of 24 June 2002 and pages 3 to 13 as originally filed,

claims: 1 to 4 filed with the fax of 24 June 2002,

drawings: Figures 1 to 9 as originally filed.

V. The claims filed with the fax of 24 June 2002 read as follows:

"1. A data management system for a programming-limited type semiconductor memory which is programmable a limited number of times and is divided into a plurality of storage blocks, each storage block including a plurality of sectors, each sector including a logical address field, a data field and an attribute management field, which indicates whether or not data in the data field of the sector may be erased, comprising:

management means for counting the number of times that programming has been performed for each of the storage blocks;

control means, coupled to said management means, for selecting one of the storage blocks for which programming has been performed the smallest number of times and for having input data written into a selected storage block, so that all the storage blocks can be equally programmed; and

means for accessing a sector by comparing a logical address contained in a read or write command with the logical addresses in the address fields of the sectors.

2. A data management system as claimed in claim 1, further comprising means for, if the command is a write command and the logical address contained in the write command does not coincide with any of the logical addresses in the address fields of the sectors, writing data contained in said write command into an idle

memory area.

3. A data management system as claimed in claim 1, further comprising means for, if the command is a write command and the logical address contained in the write command coincides with the logical address in the address field of a sector, invalidating data stored in the data field of said sector and writing data contained in said write command into an idle memory area.

4. A data management system as claimed in claim 1, wherein the programming-limited type semiconductor memory is a flash memory."

VI. The appellant essentially submitted that the features that were contained in claim 1 of the earlier application as filed were contained in the present claim 1, such that the latter, and the claims dependent on it, complied with Article 76(1) EPC.

Reasons for the Decision

1. The appeal is admissible.

2. *Article 76(1) EPC*

2.1 It is apparent that present claim 1 includes all the features that were included in claim 1 of the earlier application as filed.

Furthermore, the earlier application as filed discloses at page 9, lines 3 to 7, counting the number of times that programming has been performed.

Page 10, lines 15 to 33, of the earlier application describes the structure of data handled in the invention as comprising a plurality of storage blocks, each storage block including a plurality of sectors, each sector including a logical address field, a data field and an attribute management field, which indicates whether or not data in the data field of the sector may be erased.

It can also be deduced from the passage at page 10, line 34 to page 11, line 24 of the earlier application as filed that a sector is addressed by comparing a logical address contained in a read or write command with the logical addresses in the address fields of the sectors.

- 2.2 The feature of claim 2 is disclosed at page 11, lines 11 to 15 considered in conjunction with page 8, lines 24 to 31, the feature of claim 3 at page 11, lines 19 to 24 in conjunction with page 8, lines 24 to 31, and the feature of claim 4 at page 10, lines 16 to 20, of the earlier application.
- 2.3 Pages 1 and 2 of the present application are based on pages 1 and 2 of the earlier application as filed but have been amended to be consistent with the present claim 1 and to acknowledge prior art document US-A-4 780 855.
- 2.4 The remaining parts of the present application are identical to the corresponding parts of the earlier application as filed.
- 2.5 Therefore, the board considers that the application in its present form does not contain subject-matter which

extends beyond the content of the earlier application as filed, so that Article 76(1) EPC is not contravened.

3. *Article 123(2) EPC*

3.1 Independent claim 10 of the present application as filed was directed to a flash memory control apparatus.

However page 1, lines 8 to 19, of the description as originally filed indicates that the present invention relates to a data management system for programming-limited type semiconductor memories and, in addition to flash memories, also mentions EPROMs and EEPROMs as examples of such memories.

It is therefore apparent to the skilled person that the invention as disclosed in the application as filed is not limited to flash memories, but concerns programming-limited type semiconductor memories in general. Thus, the general reference to a programming-limited type semiconductor memory in present claim 1 is supported by the original disclosure.

3.2 The further features recited in the present claim 1 can be derived from the application as filed, in particular from page 2, lines 6 to 18, of the original description, from original claim 10 and, since pages 3 to 13 of the present application are identical to pages 3 to 13 of the earlier application, from the passages corresponding to those identified under point 2.1 above.

3.3 The features of claims 2 to 4 can be found in the passages of the present application corresponding to those identified under point 2.2 above.

- 3.4 Furthermore, pages 1 and 2 of the description have only been amended to acknowledge a prior art document and to be consistent with the present claim 1.
- 3.5 Thus, the board considers that the present application has not been amended in such a way that it contains subject-matter which extends beyond the content of the application as filed, so that Article 123(2) EPC is not contravened.
4. It appears from the file of the present application that examination, in particular as regards inventive step, has not yet been completed. Since the reasons for the refusal have been overcome, it is appropriate to remit the case to the first instance for further prosecution.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the first instance for further prosecution.

The Registrar:

The Chairman:

D. Sauter

W. J. L. Wheeler