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# D E C I S I O N
## of 29 July 2003

**Case Number:** T 0488/00 - 3.4.3

**Application Number:** 93103140.5

**Publication Number:** 0558075

**IPC:** H01L 29/04

**Language of the proceedings:** EN

**Title of invention:**
Method for fabricating a polysilicon thin film transistor

**Applicant:**
Casio Computer Co., Ltd.

**Opponent:**
-

**Headword:**
-

**Relevant legal provisions:**
EPC Art. 94, 123(2)

**Keyword:**
"Clarity and support in the description (yes)"
"Allowability of amendments (yes)"
"Inventive step (yes - after amendment)"

**Decisions cited:**
-

**Catchword:**
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**Case Number:** T 0488/00 - 3.4.3

**D E C I S I O N**
**of the Technical Board of Appeal 3.4.3**
**of 29 July 2003**

**Appellant:** Casio Computer Co., Ltd.
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**Representative:** Grünecker, Kinkedley
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**Decision under appeal:** **Decision of the Examining Division of the European Patent Office posted 27 December 1999 refusing European application No. 93103140.5 pursuant to Article 97(1) EPC.**

**Composition of the Board:**

**Chairman:** M. Chomentowski
**Members:** E. Wolff
M. B. Günzel

## Summary of Facts and Submissions

I. This is an appeal from the decision of the examining division, dated 27 December 1999, to refuse European patent application No. 93 103 140.5 on the grounds that the application did not meet the requirements of inventive step (main request) and of admissibility of amendments (auxiliary request). In respect of the main request, the decision of the examining division is based on the following prior art documents:

D1 H. Kumomi et al., Appl. Phys. Lett. 59(27), pages 3565-3567 (1991),

D2 FR-A-2573916,

D4 T. Katoh, IEEE Transactions on Electron Devices 35(7), pages 923-928 (1988),

D5 M. Sasaki et al., Appl. Phys. Lett. 49(7), 397-399 (1986).

The reasoning given by the examining division in the decision under appeal with respect to the main request which concerned a thin film transistor formed on an insulating substrate comprising a polysilicon thin film, can be summarized as follows:

All three documents D1, D4 and D5 teach that the main defects within the grains of the polysilicon are twin boundaries (micro twins) formed by the crystallites within the grains. The skilled person starting from the thin film transistor known from document D1 and trying to increase its carrier mobility would know from

documents D4 and D5 that micro twins lead to a reduced carrier mobility and need to be avoided. Accordingly, taking into account this combination of teachings, the skilled person would arrive in an obvious way at a device according to claim 1 wherein the grain size is related to the thickness of the film, and wherein the crystallite sizes are in the range of 60% or greater than 60% of the grain size, i.e. wherein crystallites and grains are of substantially the same size.

The auxiliary request concerned a method for fabricating a thin film transistor.

The examining division also stated that with respect to the method claims, the following document was relevant as prior art:

D3 Patent Abstracts of Japan, Vol. 14, No. 396, E970, June 7, 1990 & JP-A-2148831.

II. A notice of appeal was filed on 6 March 2000 and the appeal fee was paid on the same day. The statement setting out the grounds of appeal was filed on 3 May 2000.

III. In a timely response, dated 5 December 2002, to a written communication in which the Board expressed the preliminary opinion that the main and auxiliary requests filed with the statement of grounds did not appear to be allowable, the appellant filed a new request containing a new set of claims to replace the claims on the file. The appellant also requested oral proceedings should the Board intend to reach an adverse decision.

Claim 1 of the request reads as follows:

"1. A thin film transistor formed on an insulating substrate comprising a polysilicon thin-film having a middle portion for forming a channel, the polysilicon thin film formed by a laser anneal process to obtain liquid phase growth, a gate-insulating film formed on at least the middle portion on the polysilicon thin film, a gate electrode formed on the gate-insulating film, a source electrode connected to a side portion of the polysilicon thin-film, and a drain electrode connected to the other side portion of the polysilicon thin film including a plurality of grains, each of grains having a grain size c = (a+b)/2, where "a" denotes a length of each of the grains along a major axis and "b" denotes a length of each of the grains along a minor axis, the major axis and the minor axis being perpendicular to each other and parallel to the polysilicon thin film, and each grain including a crystallite having a size on the (111)-plane,

characterized in that

an average value representing the sizes on the (111) plane of said plurality of crystallites is in the range of 60% or greater than 60% of the average c of all grains included in the polysilicon thin film, said average value being at least 180 nm and being greater than a value representing the thickness of said polysilicon thin-film."

This claim, as compared to claim 1 of the main request forming the basis of the decision under appeal, additionally states in the preamble that the polysilicon thin film is formed by a laser anneal process to obtain liquid phase growth and that the major axis and the minor axis of the grains are perpendicular to each other and parallel to the polysilicon thin film.

Moreover, an average value of at least 180 nm for the grain sizes is stated, in place of 100 to 300 nm.

The further claims are dependent claims.

IV. The appellant requests that the decision under appeal be set aside and a patent be granted on the basis of claims 1 to 5 filed with the letter dated 5 December 2002. The arguments put forward by the appellant in support of the application can be summarised as follows.

The claimed polysilicon thin film transistor has a polysilicon film in which the average size of the crystallites on the (111) plane is 60% or more of the average grain size c, in which the average size of the crystallites on the (111) plane is 180 nm or more, and in which the average size of the crystallites on the (111) plane is greater than the thickness of the polysilicon thin film.

These properties distinguish the invention claimed in claim 1 from each of the cited prior art documents.

Document D1 merely describes an experimental procedure for forming polysilicon thin films but it neither relates to thin-film transistors nor does it disclose films with all of the foregoing properties.

Document D2 discloses a method of forming a polysilicon thin film in which the grain size is increased in order to provide higher field effect mobility. Document D2 is silent as regards the internal structure of the grains.

Document D3 describes a method of forming a thin film semiconductor device having a high carrier mobility, but does not refer to the internal structure of the grains and in particular not to a minimum ratio of crystallite size to grain size.

Document D4 discloses polysilicon transistors with improved characteristics on the basis that poor device characteristics are the result of defects at the grain boundaries and can accordingly be improved by using films with large grain sizes.

Document D5 relates to the formation of single-crystal silicon layers from amorphous silicon by lateral epitaxy and thus relates to subject matter completely different from the invention.

The invention claimed in claim 1 of the application in suit is therefore novel.

The object of the invention is to provide a thin film transistor with improved field effect mobility.

The solution offered by the invention is to provide a thin film transistor in which the polysilicon has the properties mentioned above in relation to novelty.

The cited documents D1, D2, D3 and D4 all point towards a solution which involves increasing grain size combined with better control of the grain boundaries (document D1), better control of the orientation of the grains (documents D2, D3) or a reduction in the number of grain boundaries (document D4). Document D5 concerns the growth by lateral epitaxy of a single crystal layer of silicon from a seeding region in a layer of amorphous silicon and is therefore not at all relevant to the present invention. Therefore, none of the cited documents, whether read alone or in combination with any of the other documents, would lead the skilled person towards seeking the looked for solution in a larger crystallite size.

The invention claimed in claim 1 of the application in suit therefore involves an inventive step.

In the amended claim 1 internal inconsistencies have been removed and previously unclear terms have been more clearly defined so that the claim now meets the requirement of clarity.

## Reasons for the Decision

1. The appeal is admissible.

2. *Clarity and support for the claims in the description (Article 84 EPC)*

The amended claim 1 overcomes the objections of lack of clarity raised by the examining division against independent device claim 1 of the main request before it (section III, point 1 of the decision). In particular, claim 1 now specifies in sufficient detail the orientation of the major and minor axes of the grains, the inconsistency regarding "in" and "on" the (111) plane has been removed, and the average crystallite size has been defined.

The Board further observes that, although central to understanding the invention, the relationship between grains and crystallites is not explicitly stated in the application. The Board nevertheless accepts that, as argued in the statement setting out the grounds of appeal, the skilled person would immediately understand from reading the description as a whole that grains are made up of one or more crystallites of approximately the same crystal orientation including crystal defects whereas crystallites are, as defined in the description (page 4, last line), "a complete monocrystal region".

The Board is therefore satisfied that the independent claim 1 of the request fulfills the requirements of Article 84 EPC.

3. *Amendments (Article 123(2) EPC)*

Claim 1 of the request differs from the corresponding claim of the application as originally filed:

(a) in that the semiconductor device of the original claim 1 is now specified to be a thin film transistor formed on an insulating substrate comprising a polysilicon thin-film having a middle portion for forming a channel,

(b) in that the polysilicon thin film is specified to be formed by a laser anneal process to obtain liquid phase growth,

(c) in that the transistor structure is set out in greater detail,

(d) in that the definition of the grain size is made explicit, including the orientation of the major and minor axes required to define the crystallite size, and

(e) the characterizing clause, introduced as such in an amendment made during examination, specifies an explicit relationship between crystallite size, grain size and thickness of the polysilicon film.

All these amendments can be derived immediately from the text and drawings, e.g. the graphs, of the application as filed, and the Board is satisfied that claim 1 of the request fulfills the requirements of Article 123(2) EPC.

4. *Novelty(Article 54 EPC)*

4.1 Claim 1 of the application in suit is to a thin film transistor in which the channel region is formed in a polysilicon thin film.

4.2 Document D4 constitutes the closest prior art. It discloses a method of fabricating polysilicon thin-film MOSFET devices, as well as the devices themselves, in which the polysilicon thin-film is a large-grain polysilicon film. Large grains reduce the number of grain boundaries in the channel region and thus lead to high carrier mobilities in the channel region. As described, a deposited fine-grain polysilicon layer is converted by ion implantation into an amorphous silicon layer. Melting and subsequent solidification of the amorphous silicon layer using laser irradiation is one of the suggested techniques (page 923, right-hand column, lines 5 to 9) for obtaining a large grain polysilicon thin-film. The device structure resulting from applying the method thus has all the features set out in the preamble of claim 1.

4.3 The claimed invention differs from the nearest prior art because the features set out in the characterizing part of the claim require that crystallites within the grains of the polysilicon layer have an average size on the (111) plane of 60% or more of the average grain size c in the polysilicon thin film and, furthermore, that the crystallites have an average size of at least 180 nm and are greater than the thickness of polysilicon thin-film.

4.4 Document D1 relates to a method of forming a thin semiconductor film with improved uniformity of the carrier mobilities. The known technique of selective nucleation based epitaxy is extended to solid state crystallisation, that is, nucleation sites in amorphous silicon are manipulated to control grain size

distribution and grain location (p. 3565, left-hand column, second paragraph). In the film produced by applying the described method, each grain has a single-crystal domain containing internal twin boundaries (p. 3565, right-hand column, second paragraph).

4.5 Document D2 relates to a method of forming a thin semiconductor film in which large grain size is achieved by annealing an amorphous semiconductor film in an inert atmosphere to obtain solid phase grain growth (page 7, lines 4 to 13; page 9, lines 13 to 20). Crystal grain size larger than the conventional grain size as well as good grain orientation (e.g., page 5, lines 4 to 13) lead to thin film transistors with improved electron mobility (e.g., page 8, lines 6 to 11) . Laser annealing is referred to but is stated to lead to polysilicon films with poor electrical characteristics (page 2, lines 24 to 35).

4.6 Document D3 relates to a method of forming a thin film semiconductor device having a large carrier mobility by irradiation with a laser to obtain a polysilicon film of (111) priority orientation and an average crystal grain size of 1000Å, i.e. 100 nm.

4.7 Document D5 relates to lateral solid phase epitaxy without discussing any particular device structures.

4.8 In view of the differences between the invention and the cited prior art, discussed also in the summary of the appellant's submissions in paragraph V above, the Board is satisfied that the invention claimed in claim 1 is new.

5. *Inventive step (Article 56 EPC)*

5.1 The examining division refused the application on the ground that the subject matter of claim 1 was obvious over a combination of documents D1, D4 and D5.

5.2 The closest prior art for the purpose of assessing whether the invention claimed in claim 1 involves an inventive step is document D4. The invention as claimed is distinguished from this prior art document by the features specified in the characterising clause of claim 1 (see paragraph 4.3 above). The technical problem solved by these features is to provide thin film polysilicon transistors with improved field effect mobility.

5.3 Document D4 identifies as the cause of the poor device characteristics of polysilicon transistors the known large number defects states at the grain boundaries, which trap carriers, become charged and lead to the formation of potential barriers (page 923, left-hand column, last paragraph, lines 1 to 4)). Two techniques are proposed as remedies. One of these is passivation with atomic hydrogen, the other is to reduce the number of grain boundaries in the channel region by using large-grain polysilicon (page 923, left-hand column, last paragraph, line 5 to right-hand column, line 7) obtained either by laser irradiation of fine-grain polysilicon or by solid state crystallisation from deposited and ion-implanted amorphous silicon. Document D4 further states that "Although a large grain size is attained, each grain has numerous defects, mainly micro twins", and that "These defects may affect the electrical characteristics of the transistors on the

poly-Si film" (page 924, right-hand column, lines 5 to 8). The Board accepts that, as argued by the appellant (statement of the grounds of appeal, page 8, second full paragraph), this indicates that the authors of document D4 attribute to the presence of these defects adverse effects on the electrical properties of the transistors in general but do not consider these defects as a relevant contribution to mobility in particular, especially since the document notes that the mobility depends strongly on the number of grain boundaries, that is, on the grain size, and the potential height at the grain boundaries. The Board therefore concludes that document D4 would not have assisted the skilled person in arriving at the subject matter of the invention as claimed in claim 1.

5.4 Document D1 relates to a method of forming thin semiconductor films with improved uniformity of the carrier mobilities. The Board agrees with the appellant (statement of the grounds of appeal, page 10, ) that the intention of document D1 is to teach that in ensuring the uniformity of carrier mobilities, enlarged grain size and control of the location of the grains and grain boundaries are essential (page 3565, left-hand column, first paragraph) and that, although the resulting grain shape is dendritic, there is nothing in document D1 which would suggest to the skilled person that the intrinsic structure of the grain as claimed in claim 1 of the application in suit has the required effect on the field effect mobility.

5.5 Document D2 relates to a method of forming thin semiconductor films with large grain sizes. The aim of increasing the grain size is to improve the electron

mobility (e.g., page 8, lines 6 to 11). The Board agrees with the appellant's submission that the document confines itself to discussing the benefits of increasing the grain size and orientation without containing any information pointing towards the essential features of the present invention as claimed in claim 1.

5.6 Document D3 relates to a method of forming a thin film semiconductor device having a large carrier mobility by irradiation with a laser to obtain a polysilicon film of (111) priority orientation and an average crystal grain size of 1000Å. In response to an objection raised by the Board on the basis of this document, the appellant has argued, in the Board's view persuasively, that the teaching in document D3 is that carrier mobility can be improved by adjusting the texture such that the (111) orientation of the grains is the preferred orientation, since in polysilicon charge carriers moving in the (111) plane experience a lower potential barrier than charge carriers moving perpendicular to that direction or charge carriers moving in a polysilicon film with randomly orientated grains, as illustrated with reference to Figure 2 of document D3 (appellant's letter of 5 December 2002, page 2). Not only does the method of obtaining the required orientation require a protective silicon dioxide layer on top of the CVD deposited silicon layer, but the grain size of the polysilicon layer in document D3 is significantly less than the thickness of the layer. Given the absence of any indication of the essential features of the invention as claimed in claim 1, it is the Board's view that document D3 neither discloses nor suggests to the skilled person

that the electron mobilities can be improved by those features.

5.7 Document D5 relates to MOS transistors fabricated on a silicon-on-insulator (SOI) region. An amorphous silicon film is converted by lateral solid phase epitaxy not into a polysilicon film but into a single crystal silicon region without any polycrystalline grains being observed (page 398, lines 11 to 16 film). Moreover, as argued by the appellant, the underlying substrate must itself be monocrystalline in order to provide the seeding for the required completely single-crystalline film on the SOI region. (page 398, lines 5 to 9). The Board therefore considers that in view of the quite different aim of the method described and the device structure resulting from the application of the method, the skilled person would not obtain any assistance from document D5 in arriving at the present invention.

5.8 Since none of the cited documents refer in any way to the relationship between grain size, crystallite size and layer thickness which is essential to the invention claimed in claim 1, and since there is no suggestion in the prior art that the appropriate choice of the ratio between average crystallite size and average grain is capable of leading to improved carrier mobilities, the Board considers that the subject matter of claim 1 involves an inventive step and thus fulfils the requirement of Articles 52(1) and 56 EPC.

5.9 Therefore, claim 1 is patentable in the sense of Article 52(1) EPC.

The further claims are dependent claims concerning particular embodiments of claim 1 and are thus patentable for the same reasons.

6. A patent can therefore be granted on this basis, with the description to be adapted thereto, if necessary.

7. Consequently, oral proceedings are not necessary.

**Order**

**For these reasons it is decided that:**

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the following documents:

**Claims:** claims 1 to 5 as filed with the letter dated 5 December 2002.

**Description:** pages 1 to 10 as originally filed, to be adapted if necessary.

**Drawings:** sheets 1/5 to 5/5 as originally filed

The Registrar: The Chairman:

D. Spigarelli M. Chomentowski