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D E C I S I O N
of 16 April 2002

Case Number: T 0369/00 - 3.5.1

Application Number: 94306625.8

Publication Number: 0644700

IPC: H04N 11/04, H03H 17/06

Language of the proceedings: EN

Title of invention:
Sampling rate converting system

Applicant:
SONY CORPORATION

Opponent:
-

Headword:
Sampling rate converter/SONY

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0369/00 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 16 April 2002

Appellant: SONY CORPORATION
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Representative: Ayers, Martyn Lewis Stanley
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 22 November 1999 refusing European patent application No. 94 306 625.8 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: S. V. Steinbrener
Members: R. R. K. Zimmermann
V. Di Cerbo

Summary of Facts and Submissions

I. European patent application No. 94 306 625.8 was filed by the appellant and relates to a system for selecting a digital signal from multi-rate signal inputs and converting it to a signal output at a predetermined sampling rate. For the invention 16 September 1993 is claimed as date of priority.

II. The examining division regarded the invention as obvious to the skilled person, in particular in view of prior art concerning the sample-rate converter chip AD1890/91 of Analog Devices Inc. (document D1: Jack Shandle, "Incompatible Audio Sources Matched by Digital IC", ELECTRONIC DESIGN 41 (1993) July 22, No. 15, Cleveland, OH (US), pages 45-50), and accordingly refused the application for lack of inventive step, with decision posted on 22 November 1999.

III. In a telex dated 14 January 2000 the appellant's representative gave notice of appeal and ordered deduction of the appeal fee from its EPO deposit account. The grounds of appeal were set out in a written statement filed on 23 March 2000.

In the course of written correspondence between the appellant and the Board, the appellant filed an amended claim 1 with a letter dated 12 March 2002, which reads as follows:

"1. An electronic appliance having a sampling rate converting system for converting the sampling rate of a digital signal, the system comprising:

a plurality of circuit blocks (1A-E) for outputting respective digital signals with respectively

different sampling frequencies, each circuit block having at least one signal output terminal (3A-E, 4A-E), a clock signal output (6A-E), and an output enable signal input (5A-E) and being adapted to output a respective one of said digital signals at the or a signal output and to output a clock signal at said clock signal output when an output enable signal is supplied to said output enable signal input (5A-E);

a parallel data bus (10,11) for commonly connecting corresponding output terminals of said circuit blocks;

a clock signal line (12) connected to the clock signal output of each of said circuit blocks;

means for supplying an output enable signal to a selected one only of the output enable signal inputs of said circuit blocks; and

a sampling rate converter (15) having an input (16,17) connected to said data bus (10,11) and said clock signal line and being adapted for converting a sampling frequency of the digital signal output by the selected circuit block and received through said data bus into a predetermined sampling frequency."

On 16 April 2002 the Board heard the appellant in oral proceedings, and announced the decision after closing the debate.

IV. The appellant regarded the invention as patentable with respect to the prior art cited by the examining division. Neither document D1 nor any other of the cited prior art documents led the skilled person in an obvious manner to the invention. Document D1, Figure 2 was a multimedia example to illustrate the use of the Analog Devices' asynchronous sample-rate converters AD1890 and AD1891, an application however which was

only very briefly explained in the document. The technical information which the examining division derived from the components shown in this figure was only available to the skilled person with *a priori* knowledge of the invention. Without hindsight the skilled person, a designer of appliances using low-cost off-the-shelf components, would end up with a completely different circuit design: a standard multiplexer did not provide the modular and easily extendable design of the invention which was achieved by using separate circuit blocks. The circuit blocks could easily be extended and adapted to the number and type of signal sources. In addition, the AD1890/91 converters required a serial data input, clearly pointing the skilled person away from using a parallel data bus. A prior art multiplexer had selection signal inputs for selecting one from a fixed number of input signals, but it would not have any kind of disconnecting function. According to the invention, however, the circuit blocks were controlled by enabling signals which disconnected the disabled circuit blocks from the data bus.

The reference book by U. Tietze et al.: "Halbleiter-Schaltungstechnik", 5th ed., Springer-Verlag Berlin Heidelberg New York 1980, of which only pages 161 and 162 were cited by the examining division, was not relevant since the text passage cited was unrelated to the problem of sampling rate conversion in electronic appliances and would thus not be consulted by the skilled person to solve the problem underlying the present invention.

V. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis

of claim 1 as filed with letter dated 12 March 2002, claims 2 to 5 as filed with letter dated 14 October 1998 and the description as amended during the oral proceedings.

Reasons for the Decision

1. The appeal complies with the requirements of Articles 106 to 108 and Rules 1(1) and 64 EPC and is thus admissible.

Furthermore, the Board is satisfied that the appellant's only request meets the requirements set out in the EPC in respect of amendments.

2. For reasons which will be explained below the invention, however, is not patentable within the meaning of Article 52(1) EPC for lack of inventive step. According to Article 56 EPC an invention shall be considered as involving an inventive step if (and only if), having regard to the prior art, the invention is not obvious to a person skilled in the art.

3. The application relates to digital video signal processing (see for example the introductory part of the description), a technical field in which the skilled person is expected to have good knowledge and competence in digital electronics and to take interest in technical publications which are, like document D1, related to this field.

Document D1 shows in Figure 2 an application for the AD1890/91 converter chip in a multimedia PC connected to networks and other audio signal sources of

incompatible data rates (see the caption text to Figure 2 of document D1). The signal sources at the input side are interconnected with the PC by an input component designated as "Receiver, ADC, multiplexer". This input component receives the inputs from the various audio signal sources and provides a "serial data" output to the data input of the AD1890 or AD1891 converter and a "serial clocks" output to the converter's "input sample clock input" (see the description of the converter chip in document D1).

Document D1, therefore, discloses an electronic appliance which converts the sampling rate of a digital signal, comprises a circuit component for outputting respective digital signals with respectively different sampling frequencies, and is adapted to output a respective one of said digital signals at the or a signal output and to output a clock signal at said clock signal output. It is also understood that the said input component comprises a data bus (the connection necessarily present for transferring the digitized audio signals to the common "serial data" output), a clock signal line (the line connecting the "serial clocks" output to the converter's "input sample clock input"), and a sampling rate converter (the AD1890/91) having an input (the converter's data and input sample clock inputs) connected (via the "serial data" line and, possibly, further output and interface circuits) to said data bus and said clock signal line and being adapted for converting a sampling frequency of the digital signal output by the input component and received through said data bus into a predetermined sampling frequency (the "programmable frequency", see document D1, Figure 2).

4. Distinguishing the invention from the said AD1890/91 application, present claim 1 specifies that the appliance comprises

a plurality of circuit blocks for outputting the digital signals, each circuit block having at least one signal output terminal, a clock signal output, and an output enable signal input and being adapted to output a respective one of said digital signals at the or a signal output and to output the clock signal at said clock signal output when an output enable signal is supplied to said output enable signal input, the clock signal line being connected to the clock signal output of each of said circuit blocks;
a parallel data bus commonly connecting corresponding output terminals of said circuit blocks, and connected to the input of the sampling rate converter; and
means for supplying an output enable signal to a selected one only of the output enable signal inputs of said circuit blocks.

5. Figure 2 of document D1, however, is a rather schematic drawing; regarding the internal circuitry of the input component, document D1 does not give any details except for showing the inputs and outputs and indicating its function as "Receiver, ADC, multiplexer". In putting the sample-rate converter chip to practical use, it is left to the skilled person as a technical problem to provide a suitable embodiment of the internal component on the basis of the sparse information given in the document.

6. Since the four audio sources shown in Figure 2 require different type of signal processing, each signal source requires a separate circuit block including a

"receiver" and/or an "ADC" for producing, at the "serial data" line, the digital audio signal format suitable for data rate conversion and, at the "serial clocks" output, a corresponding clock signal.

The digital audio signals produced by such circuit blocks have to be transmitted to a common destination point, the "serial data" output of the input component. For digital signal transmission of this kind a connection of the parallel data bus type was a normal design option in 1993. The fact that the AD1890/91 sampling rate converter has a "serial data" input is not an obstacle to the use of an internal parallel data bus within the input component since parallel-to-serial converters were state-of-the-art devices at this time.

A generally known variant of bus type connections also provided in accordance with the invention (see in particular Figures 2 and 3) interleaves the source signals on the bus by using tri-state gates, which have an enable input for switching the gate output into the high Z or high-ohm state for controlling the access of the signal sources to the bus (regarding tri-state gates as output circuits, see for example page 162, second paragraph of the reference book of U. Tietze et al.). It goes without saying that such a data bus system comprises means for producing the appropriate enable signals for the tri-state gates to output the digital audio and clock signals.

The difference between the claimed invention and said prior art appliance is thus a matter of normal design practice in the technical field and does thus not require an inventive step.

7. The appellant claimed the modular and easily extendable block structure of the inventive design to provide a considerable advantage of the invention over the prior art. Bus systems, however, normally allow to add components in a flexible and modular manner; even widening the bus width does, at least in principle, not require any modification of the circuit design. The alleged advantage over the prior art is therefore a feature typical of data bus systems rather than an indication of inventive step.

8. In summary, the subject-matter of claim 1 does not meet the requirement of inventive step. Since claim 1 was the basis of the appellant's only request, the appeal cannot be allowed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Kiehl S. V. Steinbrener