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D E C I S I O N
of 21 March 2003

Case Number: T 0352/00 - 3.4.3

Application Number: 91103412.2

Publication Number: 0449000

IPC: H01L27/108

Language of the proceedings: EN

Title of invention:

Layer structure having contact hole for fin-shaped capacitors
in DRAMS and method of producing the same

Patentee:

FUJITSU LIMITED

Opponent:

-

Headword:

Relevant legal provisions:

EPC Art. 52(1), 56

Keyword:

"Inventive step (yes)"

Decisions cited:

-

Catchword:

-



Case Number: T 0352/00 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 21 March 2003

Appellant:

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Decision under appeal:

Decision of the Examining Division of the
European Patent Office posted 26 October 1999
refusing European application No. 91103412.2
pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: R. K. Shukla
Members: E. Wolff
M. B. Günzel

Summary of Facts and Submissions

I. The appeal lies against the decision of the examining division, dispatched on 26 October 1999, rejecting European patent application Nr.91 103 412 on the ground that the subject matter of claim 1 did not involve an inventive step as required by Articles 52(1) and 56 EPC with regard to the following prior art documents

D2: IBM Technical Disclosure Bulletin, Vol. 30, No. 8, Jan 1988, pages 252 to 253;

D5: DE-A-3 916 228.

In the decision, the examining division also observed that independent device claim 23 lacked novelty with respect to document D5.

II. The notice of appeal was filed on 27 December 1999 and the appeal fee was paid on the same day. The statement setting out the grounds of appeal was filed on 25 February 2000.

III. At the oral proceedings held on 21 March 2003, the appellant replaced all previous requests with a new request for the grant of a patent on the basis of the following documents filed during the oral proceedings:

Claims: claims 1 to 48

Description: pages 1 to 5, 9 to 31 and 34

Drawings: Figures 1 to 13

The appellant also submitted a scanning electron microscope (SEM) photograph showing the detailed structure of a device as claimed in claim 22.

IV. The independent method claim 1 of the request reads as follows:

"1. A method of forming a structure having a contact hole (10, 25A, 28A, 27A), comprising the steps of:

(a) forming an insulating layer (3, 27) on a first conductive region (2, 25);

(b) forming a second conductive layer (4, 29', 46') over said insulating layer;

(c) forming an opening (6, 29A, 28A) in said second conductive layer;

(d) forming a conductive sidewall (8, 32, 47, 47a, 47b) around an inner wall of said second conductive layer defining said opening, wherein said sidewall (8, 32, 47, 47a, 47b) is formed by:

(d1) forming an additional conductive layer (32a) on the surface including the opening (6, 29A, 28A) in said second conductive layer; and

(d2) anisotropically etching said additional conductive layer (32a) to remove the horizontally extending areas of this layer (32a) and to leave behind vertically extending parts which form the sidewall (8, 32, 47, 47a, 47b);

(e) selectively etching said insulating layer in a state in which said second conductive layer and said conductive sidewall function as etching masks, so that said contact hole (10, 25A, 28A, 27A) having a width smaller than that of said opening and defined by said conductive sidewall is formed in said insulating layer and said first conductive region is exposed through said contact hole;

(f) forming a third conductive layer (17, 29", 46") on said second conductive layer, said conductive sidewall and said first conductive region being exposed through said contact hole; and

(g) patterning said third conductive layer and second conductive layer simultaneously to form a given pattern."

The independent device claim 22 of the request reads as follows:

"22. A layer structure, comprising:

a first conductive region (2, 25);

an insulating layer (3, 27) formed on said first conductive region and having a contact hole (10, 25A, 28A, 27A), said first conductive region being exposed through said contact hole;

a second conductive layer (4, 29', 46') formed over said insulating layer and having an opening

(6, 29A, 28A) having a width of approximately 0.5µm, which is the scale limit attained by the conventional photolithographic technique, and being larger than that of said contact hole, wherein said opening (6, 29A, 28A) surrounds said contact hole (10, 25A, 28A, 27A);

a conductive sidewall (8, 32, 47, 47a, 47b) formed over said insulating layer exposed through said opening and formed around an inner wall of said second conductive layer defining said opening, wherein the part of the conductive sidewall which is furthest from the second conductive layer defines the contour of said contact hole; and

a third conductive layer (17, 29", 46") formed on said second conductive layer, said conductive sidewall and said first conductive region being exposed through said contact hole."

V. The arguments put forward by the appellant can be summarised as follows.

The invention relates to the manufacture of semiconductor structures of the kind used in stacked capacitor cells. The invention aims to allow the formation of contact holes which are smaller than the size limit set by the resolution of the photolithographic processes concerned. According to the invention, a conductive layer is formed on the insulating layer to be etched and an opening is formed in the conductive layer using a conventional photolithographic process. The size of this opening is near the scale limit of the conventional

photolithographic technique. By deposition of a second conformal conductive layer and subsequent anisotropic etching, a conductive sidewall is formed inside the opening which together with the conductive layer provides a mask for etching a contact hole which is defined by the inner perimeter of the sidewall and, hence, is smaller than the opening in the conductive layer. The conductive sidewall and the conductive layer remain part of the structure of the device and therefore do not need to be removed after formation of the contact hole and before the further processing of the structure continues.

Document D5 relates to stacked capacitors and is therefore the closest prior art document. However, only conventional techniques for forming contact holes are described in document D5, which means that resolution of the lithographic processes employed sets the scale limit of features such as contact holes.

As regards claim 1, it was not disputed that the invention claimed in claim 1 is new. The claimed method is also inventive over the prior art. Starting from document D5, the problem to be solved can be considered to be the formation of holes smaller than the minimum opening attainable by photolithography. In document D2, the formation of the etching mask involves the use of materials which are insulating materials and thus different from the materials used in the invention, and these materials must, moreover, be removed by etching before processing of the structure can continue. Therefore, applying the teaching of document D2 to the fabrication of stacked capacitors known from document

D5 would not lead to the invention as claimed in claim 1.

As regards claim 22, the SEM photograph submitted provides clear evidence that the second conductive layer, the sidewall and the third conductive layer are clearly distinguishable in the finished device, contrary to the conclusion arrived at by the examining division. The structure claimed in claim 23 can thus be distinguished from the structure disclosed in document D5 and is therefore novel. Moreover, as the structure is the inevitable result of applying the inventive method claimed in claim 1, it is also in itself inventive.

Reasons for the Decision

1. The appeal is admissible.
2. *Amendments (Article 123(2) EPC)*

Claim 1

- 2.1 Claim 1 differs from claim 1 as originally filed in several respects.

The additional features

- (i) that the sidewall is formed by forming an additional conductive layer (32a) on the surface including the opening (6, 29A, 28A) in the second conductive layer (feature (d1) of claim 1),

(ii) that the additional conductive layer (32a) is anisotropically etched to remove the horizontally extending areas of this layer (32a) and to leave behind vertically extending parts which form the sidewall (8, 32, 47, 47a, 47b) (feature (d2) of claim 1) and

(iii) that the third conductive layer (17, 29", 46") is formed on said second conductive layer (feature (f) of claim 1),

are based, *inter alia*, on the originally filed description of Figures 6F to 6K on page 19, line 10 to page 20 line 35.

The additional feature that the second and third conductive layer are patterned together (feature (g) of claim 1) derives, *inter alia*, from the originally filed description of Figure 6M on page 21, lines 18 to 22.

The omission from claim 1 of the original feature (f) of "removing said second conductive layer and said conductive sidewall" is also based, *inter alia*, on the originally filed description of Figure 6H, which states that "[i]t should also be noted that the polysilicon layer 29' and the polysilicon sidewall 32 are not removed during a subsequent process, and are utilized as parts of the storage electrode of the stacked capacitor, ..." (page 20, lines 4 to 8).

Claim 22

2.2 Claim 22 corresponds to claim 23 of the application as refused by the examining division which itself was derived from claim 17 as originally filed. In substance, claim 22 differs from claim 17 in that it additionally specifies that the opening (6, 29A, 28A) in the second conductive layer (4, 29', 46')

(i) has a width of approximately $0.5\mu\text{m}$, which is the scale limit attained by the conventional photolithographic technique,

(i) is larger than, and surrounds the contact hole (10, 25A, 28A, 27A),

and that the part of the conductive sidewall which is furthest from the second conductive layer defines the contour of the contact hole.

These amendments meet the objections of lack of clarity which the Board raised in the written communication which accompanied the summons to the oral proceedings, and are all based on the description as originally filed, such as the description of Figure 6H on page 19, lines 22 to 34, for example.

The omission from the claim of the barrier layer referred to in original claim 17 is based, *inter alia*, on the embodiment of the invention which is described with reference to and shown in Figures 6H to 6K of the drawings.

2.3 *The Description*

The description has been amended by removing original Figures 3 and 15 and the accompanying description. Original Figure 3 (consisting of Figures 3A to 3D) and the associated parts of the description related to a way of obtaining the mask for forming the contact hole in a manner which is not covered by the wording of claim 1. Original Figure 15 (Figures 15A to 15J) and its associated description had as their subject a further embodiment in which a contact hole is etched through both insulating and conductive layers. Deletion of these embodiments therefore does not provide the skilled reader with information extending beyond the contents of the application as originally filed. Other amendments made to the description are merely of an editorial nature.

2.4 The Board is therefore satisfied that the amendments to the claims and description do not introduce subject matter which goes beyond the content of the application as filed and thus comply with the requirements of Article 123(2) EPC.

3. *Clarity and support (Article 84)*

3.1 Unlike claim 1 as rejected by the examining division, claim 1 now specifies that the sidewall is formed by process steps (d1) and (d2) of the claim, which is to say, by depositing a layer of conductive material and anisotropically etching that layer to leave behind vertically extending parts which form the sidewall. Inclusion of these features overcomes the objections of

lack of clarity and support raised by the Board in its written communication.

- 3.2 Claim 2, which related to the embodiment of the originally filed Figure 3 and was therefore inconsistent with the invention as now claimed in claim 1, has been deleted.
- 3.3 Claim 22, corresponding to claim 23 of the application as rejected by the examining division, now specifies that the opening in the second conductive layer is approximately 0.5 μ m wide and thus at the limit of conventional photolithography, and that the part of the conductive sidewall which is furthest from the second conductive layer defines the contour of the contact hole, thereby making it clear that the contact hole is smaller than the scale limit achievable by photolithography.
- 3.4 The Board is therefore satisfied that the claims comply with the requirements of Article 84 EPC.

4. *Novelty*

- 4.1 The novelty of the independent method claim 1 was never disputed.
- 4.2 Independent device claim 22, which corresponds to claim 23 of the rejected application, requires the presence of a second conductive layer, a conductive sidewall and a third conductive layer. The examining division considered the claim to lack novelty with respect to document D5 because the second conductive layer, the conductive sidewall and the third conductive

layer all consisted of the same material, polysilicon, and consequently were not considered as separate structures in the finished device. The claimed device could therefore not be distinguished from the structure of the device in document D5 having first and second conductive polysilicon layers which also were not discernible as separate layers in the finished device.

4.3 In the SEM photograph submitted by the appellant, however, the second conductive layer, the sidewall and the third conductive layer as claimed and described in the application are clearly visible as separate layers. As there are no reasons to doubt the authenticity of the submitted SEM photograph, the Board is satisfied that the three-component structure claimed in claim 22 can be distinguished in the finished device from the structure disclosed in document D5. Additionally, the amended claim 22 now expressly requires that the size of the opening (6, 29A, 28A) which surrounds the contact hole is at the scale limit of conventional photolithography and that the contact hole (10, 25A, 28A, 27A) is smaller than that opening. It follows that the contact hole is smaller than the scale limit of photolithography. In contrast, in the devices described in document D5 the contact holes are formed by conventional methods and cannot therefore be narrower than the scale limit of photolithography.

4.4 The Board therefore concludes that the subject matter of claim 22 is novel.

5. *Inventive step.*

5.1 *Claim 1*

5.1.1 Claim 1 relates to a method of forming a contact hole which is smaller than an opening formed by photolithography.

5.1.2 Document D5 is the closest prior art document. It relates to stacked capacitor structures for use in dynamic RAMs, and discloses a method of forming contact holes with the aid of a conventional photolithographic process. As described in column 4, lines 27 to 53 with reference to the figures following Figure 3C of document D5, an insulating layer (24) is formed, followed by a first conductive layer (30) which forms part of the first electrode of the capacitor. A conventional etching step follows to form a contact hole (26) through both the conductive layer (30) and the insulating layer (24). A second conductive layer (34), which forms a uniform film on the bottom and sides of the contact hole, is formed after the contact hole has been etched, and provides the connection to the source of the MOSFET of the memory cell concerned. Deposition of a third conductive layer constituting the second electrode of the capacitor takes place after the deposition of the insulating film (36) which forms the dielectric of the capacitor.

5.1.3 The objective problem to be solved by the invention is that already identified by the examining division, that is, to find a method of forming openings such as contact holes that are smaller in size than the minimum size of opening that can be achieved by the

conventional photolithographic technique described in document D5.

5.1.4 Document D2 discloses a method of forming holes in an insulating layer (2) smaller than the limits of conventional photolithographic techniques. The method involves the steps of depositing an insulating layer (6) on top of the insulating layer (2), forming a hole in the layer (6) by conventional lithography and depositing a further insulating layer (8) by conformal deposition. Subsequent anisotropic etching of the further layer (8) results in a vertical layer of insulating material lining the wall of the hole. The resulting aperture which forms the etch mask for the contact hole in the layer (2) is thus smaller than conventional photolithography would allow.

5.1.5 The examining division took the view that it would be obvious to apply the processing steps described in document D2 with corresponding effect to the method disclosed in document D5 (Decision, page 3, point 3.4, lines 3 to 6). To support this conclusion the examining division argued further that the skilled person would realise that the masking layer and the sidewall do not have to be removed if they are useful or required in the desired structure (point 3.4, lines 7 to 9).

5.1.6 The Board cannot share the view of the examining division. According to document D2, the etching mask is formed with the aid of two insulating layers (6) and (8). After the contact hole has been etched into the insulating layer (2) and before processing of the structure can continue, the residual material of the masking layer (6) as well as the material of the

residual vertical layer (8) need to be removed. In contrast, according to the method as claimed, the mask is formed by conductive material, the second conductive layer (4, 29', 46') and the conductive sidewall (8, 32, 47, 47a, 47b). Then, after the contact hole has been etched, the third conductive layer (17, 29", 46") is formed on both the second conductive layer and the conductive sidewall which together formed the mask. The material used as mask thus becomes a permanent part of the electrode structure of the capacitor.

5.1.7 The Board accepts the appellant's submission that there is nothing in document D2, which discloses the use of a mask formed from insulating materials deposited for the sole purpose of forming the etching mask and then removed again, to provide any incentive for the skilled person to use conductive materials as mask; nor is there any suggestion that the material used for the mask need not be removed but, instead, should remain *in situ* to form part of the finished electrode structure.

5.1.8 For the foregoing reasons, the Board concludes that the combination of documents D5 and D2 would not make the invention claimed in claim 1 obvious.

5.2 Claim 22

5.2.1 Claim 22 relates to a stacked capacitor structure. It now clearly states the opening in the second conductive layer (4, 29', 46') has a width of approximately 0.5 μ m, which is the scale limit attained by the conventional photolithographic technique, and that the contact hole is smaller than this opening, that is to say, the

- contact hole is smaller than the scale limit of conventional photolithography.
- 5.2.2 Document D5 is concerned with stacked capacitor structures and is the closest prior art with regard to claim 22. The structures disclosed have contact holes made by conventional etching techniques, which are therefore of dimensions that are within the limits set by these techniques (see, e.g., the text in column 4, lines 38 to 44, which refers to the contact holes being formed by known etching steps).
- 5.2.3 In view of the differences between the prior art structure disclosed in document D5, the objective problem solved by the invention is to provide a stacked capacitor structure in which the contact holes are smaller than the scale limit of conventional photolithography.
- 5.2.4 Document D5 gives no indication whether and, if so, how contact holes could be made smaller than the conventionally formed ones used in the structures described. The disclosure in document D2 in which the masks are provided by temporarily formed insulating layers would not provide the information necessary for the skilled person to arrive at the structure claimed in claim 22. The Board accepts the appellant's submission that the three separate conductive regions that form the contact hole, i.e. the second conductive layer (4, 29', 46'), the conductive sidewall (8, 32, 47, 47a, 47b) and the third conductive layer (17, 29", 46"), which can moreover be identified in the finished device as shown by the SEM photograph submitted by the appellant, are distinctive of the process employed for

forming the structure, and concludes that the claimed structure is not obvious from a combination of the teachings of documents D5 and D2.

- 5.3 For the foregoing reasons, in the judgement of the Board the inventions claimed in the independent claims 1 and 22 are not obvious in view of the cited prior art and hence involve an inventive step as required by Articles 52(1) and 56 EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the first instance with the order to grant a patent with the documents submitted during the oral proceedings.

The Registrar:

The Chairman:

S. Fabiani

R. K. Shukla