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**D E C I S I O N**  
**of 27 April 2004**

**Case Number:** T 0181/00 - 3.5.3

**Application Number:** 87114208.9

**Publication Number:** 0263418

**IPC:** H04Q 11/04

**Language of the proceedings:** EN

**Title of invention:**

Cross-connection network using time switch

**Patentee:**

NEC CORPORATION

**Opponent:**

ALCATEL SEL AG

**Headword:**

Cross-connection network/NEC

**Relevant legal provisions:**

EPC Art. 56

**Keyword:**

"Inventive step - no"  
"Late-filed requests (not admitted)"

**Decisions cited:**

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**Catchword:**

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Case Number: T 0181/00 - 3.5.3

**D E C I S I O N**  
of the Technical Board of Appeal 3.5.3  
of 27 April 2004

**Appellant:** NEC CORPORATION  
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Tokyo (JP)

**Representative:** VOSSIUS & PARTNER  
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**Respondent:** ALCATEL SEL AG  
(Opponent) D-70430 Stuttgart (DE)

**Representative:** Urlichs, Stefan, Dipl.-Phys.  
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**Decision under appeal:** Decision of the Opposition Division of the  
European Patent Office posted 23 November 1999  
revoking European patent No. 0263418 pursuant  
to Article 102(1) EPC.

**Composition of the Board:**

**Chairman:** A. S. Clelland  
**Members:** D. H. Rees  
R. T. Menapace

## Summary of Facts and Submissions

I. This is an appeal by the proprietor of European Patent No. 0 263 418 against the decision of the opposition division to revoke the patent.

II. Claim 1 as granted reads as follows:

"A cross-connection network having a plurality of input lines and a plurality of output lines and being operable in response to a plurality of input digital signals incoming through said input lines, said input digital signals having a first nominal bit rate in common, so as to deliver said plurality of the input signals to said output lines as a plurality of output digital signals, said network comprising: stuff and synchronization means (22) responsive to said input digital signals for carrying out pulse stuffing on said plurality of the input digital signals at a second bit rate higher than said first bit rate to produce a plurality of synchronized signals synchronized with one another, each of which includes signal bits for each of said input digital signals and extra bits different from said signal bits, said signal and said extra bits being arranged in time slots; first multiplexing means (28) responsive to said plurality of synchronized signals for multiplexing said plurality of synchronized signals into at least one multiplexed signal, each of said at least one multiplexed signal having a plurality of frames assigned to said plurality of synchronized signals, each of said plurality of frames having bit signals in each one of said plurality of synchronized signals assigned thereto, each of said plurality or (sic) frames being also assigned to said plurality of

output lines; exchanging means (31) operable in a time division fashion for exchanging said frames to one another in said at least one multiplexed signal to produce at least one exchanged multiplexed signals (sic) after exchanging said frames; first demultiplexing means (33) coupled to said exchanging means (31) for demultiplexing said at least one exchanged multiplexed signal into a plurality of demultiplexed signals having said bit signals in said frames, respectively; and destuff means (35) responsive to said plurality of demultiplexed signals for producing said plurality of output digital signals by removing said extra bits from said plurality of demultiplexed signals, each one of said plurality of output digital signals being delivered to each one of said plurality of output lines assigned with one of said frames corresponding to said each one output signal, wherein serial-to-parallel converting means (26) is coupled to said stuff and synchronization means (22) for converting each of said plurality of synchronized signals from a bit serial form into a bit parallel form; said first multiplexing means (28) coupled to said serial-to-parallel converting means (26) and multiplexing said plurality of bit-parallel synchronized signals to produce a plurality of said multiplexed signals as said at least one multiplexed signal; said exchanging means (31) producing a plurality of exchanged multiplexed signals as said at least one exchanged multiplexed signal after exchanging said frames in said plurality of multiplexed signals; said first demultiplexing means (33) demultiplexing respective exchanged multiplexed signals to produce said plurality of demultiplexed signals each of which is a bit-parallel signal; and parallel-to-serial

converting means (34) is coupled to said first demultiplexing means (33) for converting each of said plurality of demultiplexed signals from the bit parallel form into the bit serial form, said plurality of demultiplexed signals being supplied to said destuff means (35) after each converted into the bit-serial form."

III. The opponent (respondent) had requested the revocation of the patent on the grounds that the invention lacked an inventive step with respect to the disclosure of the documents

D1: US-A-3 971 891 and

D2: E. Hölzer et al., "Pulstechnik Band II Anwendungen und Systeme," pages 355 to 366, Berlin, Springer Verlag, 1976.

IV. In oral proceedings held 25 October 1999, the opposition division found that the subject matter of granted claim 1, and of claim 1 of an auxiliary request (referred to in this decision as Auxiliary Request A) did not involve an inventive step having regard to a combination of documents D1 and D2. Claim 1 of Auxiliary Request A reads as follows:

"A cross-connection network having a plurality of first to n-th input lines (20) and a plurality of first to n-th output lines (21) and being operable in response to a plurality of input digital signals incoming through said input lines, said input digital signals having a first nominal bit rate in common, so as to deliver said plurality of the input signals to said output lines as

a plurality of output digital signals, said network comprising: stuff and synchronization means (22) responsive to said first to n-th input digital signals for carrying out pulse stuffing on said plurality of the input digital signals at a second bit rate higher than said first bit rate to produce a plurality of first to n-th synchronized signals synchronized with one another, each of which includes m signal bits for each of said input digital signals and extra bits different from said signal bits, said signal and said extra bits being arranged in time slots; first multiplexing means (28) responsive to said plurality of first to n-th synchronized signals for multiplexing said plurality of synchronized signals into a multiplexed signal, said multiplexed signal having a plurality of frames assigned to said plurality of first to n-th synchronized signals, each of said plurality of frames having bit signals in each one of said plurality of first to n-th synchronized signals assigned thereto, each of said plurality of frames being also assigned to said plurality of first to n-th output lines; exchanging means (31) operable in a time division fashion for exchanging said frames to one another in said multiplexed signal to produce an exchanged multiplexed signals after exchanging said frames; first demultiplexing means (33) coupled to said exchanging means (31) for demultiplexing said exchanged multiplexed signal into a plurality of first to n-th demultiplexed signals having said bit signals in said frames, respectively; and destuff means (35) responsive to said plurality of first to n-th demultiplexed signals for producing said plurality of first to n-th output digital signals by removing said extra bits from said plurality of demultiplexed signals, each one of

said plurality of first to n-th output digital signals being delivered to each one of said plurality of first to n-th output lines assigned with one of said frames corresponding to said each one output signal, wherein serial-to-parallel converting means (26) is coupled to said stuff and synchronization means (22) for converting each of said plurality of first to n-th synchronized signals from a m-bit serial form into a m-bit parallel form; said first multiplexing means (28) is coupled to said serial-to-parallel converting means (26) and multiplexes said plurality of first to n-th m-bit-parallel synchronized signals to produce a plurality of first to m-th multiplexed signals each comprising n serial bits; said exchanging means (31) exchanges said frames in said plurality of first to m-th multiplexed signals to produce a plurality of first to m-th exchanged multiplexed signals; said first demultiplexing means (33) demultiplexes respective first to m-th exchanged multiplexed signals to produce a plurality of first to n-th demultiplexed signals each of which is a m-bit-parallel signal; and parallel-to-serial converting means (34) is coupled to said first demultiplexing means (33) for converting each of said plurality of first to n-th demultiplexed signals from the m-bit parallel form into the m-bit serial form, said plurality of first to n-th demultiplexed signals being supplied to said destuff means (35) after each converted into the m-bit-serial form."

The written decision revoking the patent was dispatched on 23 November 1999.

- V. Notice of appeal was filed, with the appropriate fee, on 1 February 2000. A statement of grounds of appeal,

reiterating the main request and Auxiliary Request A, was submitted on 3 April 2000. The respondent submitted arguments on 21 August 2000, requesting dismissal of the appeal. The appellant made further observations on 1 March 2001.

VI. On 10 February 2004 the appellant submitted a new Auxiliary Request B, based on a new claim 1 derived from the granted claim 1 by replacing "each of said plurality of frames having bit signals" by "each of said plurality of frames having a frame pulse time slot, data bit time slots, vacant bit time slots, stuff control bit time slots and a parity bit time slot."

With a letter received on 26 February 2004 the respondent cited a new document

D5: US-A-4 543 652.

While maintaining the arguments previously made, based on a combination of D1 and D2, the respondent argued that the main claim as granted also lacked an inventive step based on D5 and D1, and that auxiliary requests A and B did not overcome these objections.

On 16 April 2004 the appellant submitted a further request, Auxiliary Request C, based on a new claim 1 derived from granted claim 1 and additionally limited by the following features:

"wherein the cross-connection network is also operable in response to the input digital signals of another nominal bit rate that is different from the first



nominal bit rate to be stuffed at the second bit rate higher than another nominal bit rate."

At the oral proceedings held on 27 April 2004, after the main request and auxiliary requests A to C had been discussed, the appellant submitted Auxiliary Request D, based on the granted claim 1 and additionally limited by the following features derived from granted dependent claim 4, the other claims to be renumbered appropriately:

"wherein the said stuff and synchronization means (22) comprises:

a plurality of second demultiplexing means (51) responsive to said plurality of the input digital signals each of which is of a higher order group, each of said demultiplexing means (51) being for demultiplexing said input digital signals into a plurality of intermediate digital signals each of which is a lower order group; and  
a plurality of pulse stuffing and multiplexing means (52) coupled to the respective second demultiplexing means (51) for multiplexing the respective intermediate digital signals into said synchronized signals by attaching said extra bits to the respective intermediate digital signals."

- VII. The appellant requested the maintenance of the patent on the basis of the main or one of Auxiliary Requests A to D.
- VIII. The respondent requested that the appeal be dismissed.
- IX. The decision of the board was announced at the end of the oral proceedings.

## Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.
2. *Admissibility of the auxiliary requests.*
  - 2.1 Claim 1 of Auxiliary Request A refers to a plurality of synchronised signals "each of which includes m signal bits for each of said input digital signals and extra bits different from said signal bits". By comparison with the description (page 4, lines 16 to 20, and lines 28 to 36 of the published patent), and when considering the consequential features specified in the claim, for example "for converting each of said plurality of first to n-th synchronized signals from a m-bit serial form into a m-bit parallel form," it would appear that a frame should consist of m bits in total, rather than, as literally claimed, m signal input bits plus extra bits added by the stuffing process. The board therefore interprets this feature as requiring m bits in total and sees no reason to question the admissibility of the request, which only differs from the main request in specifying the degree of parallelisation carried out, see the published application as filed at page 4, lines 20 to 23. Nor was any objection raised in the appeal by the respondent to the admissibility of this request.
  - 2.2 Claim 1 of Auxiliary Request B merely specifies more precisely what a frame consists of, the frame as such being a feature of the granted independent claim. This

amendment finds a basis in the application as originally filed (see page 5, lines 33 and 34, of the published application). Again, no objection was raised by the respondent. It is, therefore, admitted.

- 2.3 Auxiliary Request C was late filed, having been received by the board only eleven days before the oral proceedings. When claim 1 was discussed in the oral proceedings, it became apparent that it was not possible to identify an input signal in the described embodiments which could correspond to the "input digital signals of another nominal bit rate" now claimed. Moreover, on the basis of a preliminary interpretation the board understands the new claim as specifying a single "cross-connection network" which could, without change, handle input signals of two different nominal bit rates. However, there appears to be no clear and unambiguous disclosure of such a device, as opposed to a device which could be adapted to different nominal bit rates or a number of different devices which could be built to deal with different nominal rates and formats. The appellant has pointed to page 6, lines 49 to 51, and page 7, lines 51 and 52 of the published patent, and the corresponding figures, but the board does not find that these provide the required clear and unambiguous disclosure.

In view of these manifest potential objections to the new claim, this late filed request is not clearly allowable and thus, in line with the consistent jurisprudence of the boards, not admitted.

- 2.4 Auxiliary Request D was submitted towards the end of the oral proceedings, when all other requests had been

discussed. It appears that the new claim 1 merely adds to claim 1 of the main request the feature of demultiplexing a "higher order group" signal before switching its "lower order group" contents individually, a process which would be necessary if for example an individual call from an incoming trunk line was to be delivered to a local loop; it appears that this may be done in the apparatus of D1 (Figure 1, trunk input 153 and loop output 144), so that the added feature *prima facie* seems unlikely to make an inventive contribution to the art. A thorough assessment of this new claim would however require a review of documents not yet discussed in the appeal as well as hearing full arguments from both parties. Thus, this very late request cannot be considered clearly allowable, and is therefore inadmissible.

3. *Inventive step (main request)*

3.1 D1 discloses (reference numbers taken from Figure 1): A cross-connection network having a plurality of input lines ("CVSD loop", 146) and a plurality of output lines (145) and being operable in response to a plurality of input digital signals incoming through said input lines, said input digital signals having a first nominal bit rate in common ("32 kilobits per second per CVSD channel" - D1 column 3, lines 18 and 19), so as to deliver said plurality of the input signals to said output lines as a plurality of output digital signals, said network comprising: stuff and synchronization means responsive to said input digital signals for carrying out pulse stuffing on said plurality of the input digital signals at a second bit rate higher than said first bit rate to produce a

plurality of synchronized signals synchronized with one another ("loop input sync", 159, column 13, lines 59 to column 14, line 6), each of which includes signal bits for each of said input digital signals and extra bits different from said signal bits (column 13, line 66, to column 14, line 6), said signal and said extra bits being arranged in time slots; first multiplexing means (141) responsive to said plurality of synchronized signals for multiplexing said plurality of synchronized signals into at least one multiplexed signal, each of said at least one multiplexed signal having a plurality of frames (column 13, line 66, to column 14, line 6, again) assigned to said plurality of synchronized signals, each of said plurality of frames having bit signals in each one of said plurality of synchronized signals assigned thereto, each of said plurality of frames being also assigned to said plurality of output lines (column 14, lines 19 to 22, "Therefore, each loop must be separately ... destuffed in the ... output loop synchronizer circuits 160,"); exchanging means (124, 127) operable in a time division fashion for exchanging said frames to one another in said at least one multiplexed signal to produce at least one exchanged multiplexed signal after exchanging said frames; first demultiplexing means (140) coupled to said exchanging means (124, 127) for demultiplexing said at least one exchanged multiplexed signal into a plurality of demultiplexed signals having said bit signals in said frames, respectively; and destuff means (160) responsive to said plurality of demultiplexed signals for producing said plurality of output digital signals by removing said extra bits from said plurality of demultiplexed signals, each one of said plurality of output digital signals being delivered to each one of

said plurality of output lines assigned with one of said frames corresponding to said each one output signal.

Thus the only features specified in claim 1 of the main request and not disclosed in D1 are the serial-to-parallel and parallel-to-serial converting means.

3.2 D2 is a textbook published ten years before the priority date of the disputed patent. The presentation of Chapter 9 is in a form typical of an introductory text on its subject, which is (in translation), "Digital switches and integrated networks." The board considers therefore that its contents are a fair reflection of information which the person skilled in the art of digital switch design would possess as background knowledge, and that the skilled person would apply the teachings to be found in this document according to the general principles it lays out without requiring any specific spur from the starting point for development, in this case document D1.

3.3 At lines 5 to 7 of page 360, D2 states (the board's translation), "If the information of the channel consists of several bits - as in PCM - an initial serial-parallel conversion is often carried out." Reference is further made to Figure 9.9 on the same page, which shows the specific case of a full serial-parallel conversion, where all the bits belonging to one channel entry are dealt with in parallel. On page 361, lines 1 and 2, it is explained that by carrying out such a conversion time is gained, which statement the skilled person would understand to mean that either slower, cheaper components could be used,

or the capacity of the switch could be increased for a given maximum speed of the components used. Again, in the following lines this principle is illustrated using full serial-parallel conversion. The board considers also that the skilled person would appreciate that serial-parallel conversion also multiplies the number of lines and components necessary, so that in fact the question of whether or not to use serial-parallel conversion is a trade-off.

3.4 In the case of D1, the process of stuffing creates frames (D1, column 13, line 66, to column 14, line 6), and it is clear that the whole of such a frame must be switched to a single output, in order that it can be destuffed (column 14, lines 19 to 22). Hence, the frame forms a channel (entry) in the sense used in D2. Therefore the skilled person would be motivated to apply the teaching of D2 to these frames, to gain the advantages discussed above.

3.5 The appellant has argued that even if the skilled person were to apply the teaching of D2 to D1, this would not lead to the claimed subject-matter, since the serial-parallel converters could be between the multiplexer and the "exchanging means". The board accepts that this would be theoretically possible. However, this would mean that the benefits in using lower speed components or having higher capacity would be confined to the exchanging means. In the view of the board it would be more probable that the skilled person would place the serial-parallel converters before the multiplexers, with the resultant evident benefits. Hence the board considers it obvious to couple serial-to-parallel converting means to the stuff and

synchronisation means and the multiplexing means of the apparatus of D1, and parallel-to-serial means to its demultiplexing means and its destuff means. In this way the skilled person would arrive without inventive activity at the subject-matter of the independent claim of the main request.

4. *Inventive step (auxiliary requests A and B)*

4.1 The only further restriction on the claimed subject-matter imposed by the amendments made in Auxiliary Request A is that the parallel output of the serial-parallel converters has the same width as a frame has length, i.e. that full serial-parallel conversion is carried out. While there are other possibilities, this would be the first option that the skilled person would contemplate, noting that full serial-parallel conversion is also used in the examples given in D2. Thus the subject-matter of claim 1 of this auxiliary request also lacks an inventive step.

4.2 The independent claim of Auxiliary Request B differs from granted claim 1 in that it specifies that frames have "a frame pulse time slot, data bit time slots, vacant bit time slots, stuff control bit time slots and a parity bit time slot." D1 states that stuffing takes the incoming signal and adds "frame bits which enable the stuffed bits to be detected, a rate adjustment bit which may contain either a valid signal bit or a stuffed bit, and a code word which identifies the rate adjustment bit as either valid or stuffed." Bearing in mind that the precise format of a frame depends not only on the bits added in the stuffing process (specified in the description as "a frame bit, at least



one stuff bit, and a stuff control bit" - page 4, lines 28 to 30, of the published patent) but also on the format of the signal being stuffed, which is otherwise irrelevant to the subject-matter claimed, the difference between these definitions does not reflect any inventive contribution to the art, and nor is there any synergistic interaction with the other features. Therefore the subject-matter of this claim also lacks an inventive step.

5. Hence none of the appellant's admissible requests are allowable.

## **Order**

### **For these reasons it is decided that:**

The appeal is dismissed.

The Registrar:

The Chairman:

D. Magliano

A. S. Clelland