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D E C I S I O N
of 13 February 2002

Case Number: T 0019/00 - 3.5.2

Application Number: 93912342.8

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Language of the proceedings: EN

Title of invention:
Self-compensating voltage level shifting circuit

Applicant:
Compaq Computer Corporation

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (main request no)"
"Remittal (auxiliary request)"

Decisions cited:
-

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Case Number: T 0019/00 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 13 February 2002

Appellant: Compaq Computer Corporation
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 8 July 1998 refusing European patent application No. 93 912 342.8 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: F. Edlinger
B. J. Schachenmann

Summary of Facts and Submissions

I. This appeal is against the decision of the examining division refusing European application No. 93 912 342.8 (published as International application WO 93/22837).

II. In response to the summons to oral proceedings before the Board, the appellant filed claims 1 to 5 (main request) and claims 1 to 3 (auxiliary request) with letter dated 11 January 2002. Following a telephone conversation between the appellant's representative and the rapporteur of the Board, the appellant confirmed with fax dated 12 February 2002 that he would not attend the oral proceedings scheduled for 13 February 2002.

III. The Board held oral proceedings as scheduled on 13 February 2002 in the absence of the appellant.

IV. Claim 1 of the main request has the following wording:

"A voltage level shifting circuit (200) for shifting first and second voltage levels of a first device to respective first and second shifted voltage levels of a second device, the circuit comprising:

in the first device (A, 202) and coupled to a first power supply (210-211) thereof, a trigger circuit (206-216) having an input (204) for receiving the first and second voltage levels, and

in the second device (B, 218), and coupled to a second power supply (220,226) thereof, a first shifted voltage level supply means (222-228) and a second shifted voltage level supply means (232-238);

output means (242-246), adapted to provide said first and second shifted voltage levels at an output thereof;

the trigger circuit (206-216) comprising:

first switch means (208), connected to the input (204), for providing a first voltage signal to a first line (212) when the second voltage level is provided at the input;

second switch means (206), connected to the input (204), for providing a second voltage signal to the first line (212) when the first voltage level is provided at the input;

third switch means (214) connected to the first line (212) responsive to the first voltage signal for connecting said first shifted voltage level supply means (222-228) to said output means (242-246); and

fourth switch means (216) connected to the first line (212) responsive to said second voltage signal for connecting said second shifted voltage level supply means (232-238) to the output means."

Claims 2 to 5 are dependent on claim 1.

V. Claim 1 of the auxiliary request, except for missing reference signs in lines 11 and 20, has the same wording as claim 1 of the main request and adds the following features after "output means" at the end thereof:

"and wherein each of the first and second shifted voltage level supply means includes resistive voltage

divider means (222, 224; 232, 234) coupled between the second power supply (220) and a ground reference (226), and a buffer amplifier (228, 238) for providing the shifted voltage level to said respective third and fourth switch means."

Claims 2 and 3 are dependent on claim 1.

VI. The reasons for refusing the present application given in the decision under appeal may be translated into the new claim language and summarised as follows, in so far as they apply to the subject-matter of the amended claims:

WO-A-87/03758 (document D1, page 2, last paragraph) related to the same problem as the present application. The trigger circuit of D1, Figure 1, included first and second switch means (which were invariably comprised in CMOS logic circuit 12 and shared a common input) as well as third and fourth switch means (14, 16). A first shifted voltage level from a first shifted voltage level supply means (Q3 etc) or a second shifted voltage level from a second shifted voltage level supply means (Q4 etc) was provided at an output means (Vo). D1 lacked an explicit circuit diagram of the output stage of the CMOS logic circuit (12). In the absence of any contrary teaching, the person skilled in the art would select a standard form of a CMOS stage as a routine choice, and would thus arrive at the subject-matter of claim 1 without involving an inventive step.

VII. The appellant essentially argued as follows:

When devices A and B of different logic families were coupled together, it was necessary to convert the logic

levels. The converted logic levels varied with transient and thermal variations of both devices A and B. The inventor of the present application had recognised that it was necessary to provide various degrees of isolation from these variations by providing, in a first device A, a two-stage trigger circuit comprising first to fourth switch means. The first and second switch means provided a voltage signal to the third and fourth switch means which had significantly less voltage variation than the input signal. The third and fourth switch means merely acted as transmission gates for signals generated within device B and thus subject to all the conditions of temperature etc existing in device B.

D1 related to a different problem of ensuring that the shifted voltage level automatically tracked variations arising from temperature changes in the ECL logic circuit. D1 was completely silent about the need for providing isolation from the conditions existing within device 10. There was no motivation to provide a second stage in a trigger circuit to provide a further degree of isolation. Although it was common general knowledge that transistors in CMOS integrated circuits were arranged with their main current paths connected in series chains, the configuration of these transistors could vary greatly (eg OR, NOR, XOR functions), and D1 contained no teaching towards the specific configuration, nor towards the benefits and desirability of providing the two-stage trigger circuit, of the present application. The decision under appeal merely alleged, but did not demonstrate, that CMOS logic circuit output stages invariably comprised a pair of series connected PFET and NFET that would provide a direct equivalent to the first and second

switch means of the present application.

In accordance with established jurisprudence of the boards of appeal, the question to be decided was not whether the person skilled in the art could have arrived at the subject-matter as claimed considering the technical feasibility and the absence of obstacles, but whether the skilled person would have done so. It was thus necessary to show that there was a recognisable pointer in the prior art to combine known means and the conventional device. The person skilled in the art did not act out of idle curiosity but with a specific technical purpose in mind. Since there was no motivation in D1 to improve the degree of isolation, there was also no suggestion that a second stage of the trigger circuit was needed or desired. D1 (page 3, lines 17 to 22) rather pointed away from this solution in that it mentioned the possibility of forming the third and fourth switch means (14, 16) as part of the CMOS logic device 10. When utilising the circuit of D1 in connection with a logic circuit that had already been designed to include a series-connected CMOS pair output stage, it was more likely to use these two existing output stage transistors as the third and fourth switch means (merely changing their supply rails to V_A and V_B) than add two further transistors. This would constitute a preferred implementation of the prior art circuit because of the saving in silicon real estate. Therefore, D1 did not offer any prompting towards a two-stage trigger circuit and the person skilled in the art would not have arrived at the subject-matter of claim 1 of the main request without involving an inventive step.

Claim 1 of the auxiliary request specified a more

accurate means of establishing a voltage level than the emitter-base diode of a bipolar transistor as disclosed in D1. A resistive voltage divider and buffer were not suggested by D1 and, despite the disadvantage of occupying more space on a chip, offered a substantially simplified circuit configuration which could be advantageously used in certain types of logic family.

VIII. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of claims 1 to 5 (main request) filed with letter dated 11 January 2002, or claims 1 to 3 (auxiliary request) filed with letter dated 11 January 2002, or that the case be remitted to the first instance for consideration of the auxiliary request.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request*

2.1 D1 (Figure 1, abstract) discloses a voltage level shifting circuit for shifting first and second (CMOS) voltage levels of a first device (10) to respective first and second shifted (ECL) voltage levels of a second device, ie the device comprising the ECL logic gates, in particular any of the "other ECL logic fan out" (D1, Figure 1) which constitute "serviced ECL devices" (D1, page 1, first full paragraph; page 3, lines 12 to 14). The circuit comprises, in the first device and coupled to a first power supply (V_{cc}, V_{ss}) thereof, a trigger circuit (including CMOS logic circuit 12 and switches 14 and 16) having an input for

receiving the first and second voltage levels (at least one input would be an inherent feature of any CMOS "logic circuit"). First and second shifted voltage level supply means (Q3, Q4, etc) are coupled to a second power supply and comprised in the second device (device 20, "by using one of the unused ECL logic gates", is located in the same second device and "exposed to the same temperature environment as the other ECL logic gates"; D1, page 4, paragraph 1). Output means (line connected to the common output node of switches 14 and 16 supplying signal V_0 to other ECL logic fan out) are adapted to provide said first and second shifted voltage levels at an output thereof (D1, pages 3 and 4, bridging paragraph). Third switch means (14) connected to a first line (common input to switches 14 and 16) are responsive to a first voltage signal (eg V1L) for connecting said first shifted voltage level supply means (eg Q3) to said output means; and fourth switch means (16) connected to the first line are responsive to a second voltage signal (eg V1H) for connecting said second shifted voltage level supply means (eg Q4) to the output means (see D1, Figures 1 and 2; page 5, paragraphs 1 and 2).

2.2 By deriving its power from (an unused ECL logic gate of) the second device located in the same temperature environment as the serviced ECL logic devices (and not from the power supply of the first device 10), the level shifting circuit of D1 (page 1, second paragraph; page 2, last paragraph; pages 3 and 4, bridging paragraph) isolates the serviced ECL logic devices of the second device, with respect to the valid logic level, from the conditions (temperature and voltage induced signal shifts) existing in the first device. As in the case of the third and fourth switch means (214,

216) of the present application (Figure 3), the third and fourth switch means of D1 act as transmission gates, triggered by a logic signal at the first line, for signals generated and subject to all the conditions within the second device. These switch means therefore constitute a part of a trigger circuit in the meaning of the present application.

2.3 D1 does not disclose any details of the structure of the logic circuit 12, but it constitutes common general knowledge that transistors in CMOS integrated circuits are arranged with their main current paths connected in series chains so that one transistor tends to turn on while its complement is turning off. First and second switch means, connected to at least one input, for providing first and second (logic) voltage signals to the first line, respectively, would therefore be invariably present in any CMOS logic circuit as disclosed in D1. The levels of the voltage signals (V1) provided to the first line vary according to the voltage-transfer characteristic of the CMOS logic circuit and thus provide a certain degree of isolation between the corresponding inputs and outputs of the first and second switch means, as in the preferred embodiment of the present application (Figure 3) where the first and second switch means have a common input.

2.4 However, the configuration of the transistors of a CMOS logic circuit (shown as block 12 in D1), in particular the connection of their respective gates with the at least one input, may vary greatly to achieve the logic functions and input/output characteristics which are desired for a specific use. Therefore, the subject-matter of claim 1 of the main request differs from the voltage level shifting circuit disclosed in D1 in that

the first and second switch means in D1 (which are implicit in the CMOS logic circuit 12) are not necessarily so connected that the first switch means, connected to the input, provides a first voltage signal to the first line when the second voltage level is provided at the input, and the second switch means, connected to the (same) input, provides a second voltage signal to the first line when the first voltage level is provided at the (same) input.

2.5 It follows from the foregoing that the problem of isolating the second device from temperature and voltage induced signal shifts of the first device, mentioned in the application as published (page 6, lines 14 to 17; page 12, lines 5 to 10), is already solved in D1 and therefore may not serve as the objective problem when D1 is used as a starting point. In view of the differences mentioned in the preceding paragraph, the Board considers that the objective technical problem underlying the subject-matter of claim 1 consists in filling the gaps left in the disclosure of D1 for reducing its teaching to practice in accordance with the specific requirements of the logic circuits of the first and second devices for a given purpose.

2.6 Filling these gaps in the way as specified in claim 1 of the main request constitutes a matter of routine choice. A basic CMOS inverter for inverting a logic signal, or an additional CMOS output buffer stage having a common input for increasing the current gain at the output of the logic circuit, would constitute elements readily contemplated by the person skilled in the art to achieve the logic functions and input/output characteristics which are desirable in the

circumstances of a given use. The series connected CMOS transistors of such routine embodiments of the CMOS logic circuit 12, in combination with the switches 14 and 16 would form a trigger circuit where a first voltage signal (eg H) is provided to the first line when a second voltage level (eg L) is provided at the input of the trigger circuit (the common input of the CMOS inverter or buffer), and where a second voltage signal (eg L) is provided to the first line when the first voltage level (eg H) is provided at the input of this trigger circuit.

2.7 The mentioning of an "interfacing circuit, comprised of complementary field effect transistors 14 and 16, which may be formed using discrete devices or as part of the CMOS logic device 10" (D1, page 3, lines 19 to 24) does not teach away from using first and second switch means in the CMOS logic circuit 12 in combination with third and fourth switch means. First, it should be noted that this passage refers to a part of the logic device 10, as a whole, not to a part of the CMOS logic circuit 12 to which the considerations mentioned in paragraphs 2.3 to 2.6 above apply. Second, if these transistors were integrated in one and the same CMOS logic circuit, their drain-source current paths would nevertheless have to be coupled to the power supply in the second device which provides the first and second shifted voltage levels. They would thus be differently connected (and have to comply with different requirements) than two existing output stage transistors of the CMOS logic circuit 12, which would be connected with their drain-source paths to the CMOS power supply of the first device. Nothing else is disclosed for the third and fourth switch means (214, 216) of the trigger circuit of the present

application. The feature of claim 1 specifying that the trigger circuit is "coupled to a first power supply" of the first device does not mean that the drain-source paths of the third and fourth switch means are connected to the first power supply (cf Figure 3).

2.8 The Board does not agree that such modifications of the circuit disclosed in D1 merely represent a possibility, considering the technical feasibility and the absence of obstacles, of what a person skilled in the art could have done, but that he had no motivation to do it. The adaptation of a known level shifting circuit to the circumstances of a given use as set out above is part of the routine work of a person skilled in the art. It thus constitutes a concrete technical reason for which a person skilled in the art would modify or supplement the technical teaching of D1 with known means to satisfy requirements arising from the circumstances of the given use. Since a person skilled in the art may be assumed to carry out such obvious modifications as part of his routine work, it is not necessary for there to be an additional recognisable pointer in the prior art to combine a particular known means with a conventional circuit. Therefore, the subject-matter of claim 1 of the main request represents an obvious modification of the level shifting circuit disclosed in D1 and cannot be considered as involving an inventive step (Article 56 EPC). The main request thus has to be refused.

3. *Auxiliary request*

The additional features of claim 1 of the auxiliary request relating to a resistive voltage divider means and a buffer amplifier relate to a different aspect of

the level shifting circuit, namely that of how the shifted voltage levels are produced. Such features were present in dependent claims 4 and 5 on file when the decision under appeal was taken, but not dealt with in that decision, nor in the preceding examination. The Board does not wish to comment on this subject-matter so as not to preempt the examination of the first instance on this request, and decides, pursuant to Article 111(1) EPC, to remit the case to the examining division for further prosecution.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The main request is refused.

3. The case is remitted to the first instance for further prosecution.

The Registrar: The Chairman:

M. Hörnell W. J. L. Wheeler